EM62100

65 COM/ 132 SEG STN LCD Driver

Product Specification

DOC. VERSION 1.1

ELAN MICROELECTRONICS CORP.

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Contents

Specification Revision History

Doc. Version	Revision Description	Date
0.1	Preliminary version	2005/05/05
0.2	1. Modified the interface type selection table (table2) 2. Modified the parallel interface table (table3) 3. Pins renamed: VDD2→VCI, RW→R/WB, C86→M86, P_S→P/S, CLS→CKS, CL→CK, FR→M, FRS→FLM 4. Added Pin coordinate table in Pin configuration on page 4 ~ 7	2005/05/10
0.3	1. Modified the Pin Coordinate Table (pin 71 ~ pin 78 X coordinate) on page 4 2. Added Alignment Key (A1, A2) to Pin Configuration table on page 3 3. Deleted Part No. EM62100AU, EM62100BU from the Package table on page 3 4. Modified VDD, VDD2, VSS, VSS2,VSS3 function in Pin Description on page 7 5. Pins renamed: D0 to D7→ D0, D1, D2, D3, D4, D5, D6 (SCL), D7 (SI), R/WB→RW, on page 8, VCI → VEE and modified the VEE pin function description on page 10 6. Deleted 6.12.4 voltage follower down control 7. Modified 6.13.1 item mark and Added 6.13 description on page 25 8. Added section 7. Command Register & Decoder description on page 26 9. Modified the Command Function Table E RDB → RDB , R/W WRB →WRB 10. Modified section 7.2.5 Read status table: RDB=1, WRB=0 → RDB=0 , WRB=1 on page 31 11. Modified section 7.2.16 Power Control Set table: A2, A1, A0 → VB, VR, VF on page 35 12. Modified section 9 DC Characteristics: Hz → Hi-z on page 38 , VOUT`1 ~VOUT4 MAX RATING 5XVDD2X0.99 ~ 2XVDD2X0.99 → 5XVDD2 ~ 2XVDD2 13. Added No. of pins in Pin Description table on pages 7 ~ 10 14. Added Pin Configuration on page 2 15. Added sections 3.1 Pin Dimensions , 3.2 Mark Dimensions, 3.3 Alignment Key on page 3 16. Modified Pin Description: swapped Pin names CAP1± ; CAP2±	2005/06/15
1.0	1. Added Timing rating to AC Characteristics table on page 49~52. 2. Added be take notice of item in serial mode on page 51 3. Added f_{FRM} rating and Base Voltage rating to AC Characteristics table on page 47~48. 4. Modified VREF pin input only and the function in Pin Description on page 7 5. Added Current consumption to DC Characteristics table on page 47	2005/8/16

1.1	1. Modified I_{SB} MAX. rating =10 uA	2005/09/13

1 General Description

The EM62100 is a 65 Common 132 Segment dot matrix liquid crystal display (**LCD**) driver LSI. It can be connected directly to a microprocessor bus, and selected as an 8-bit parallel or serial data input interface. The EM62100 IC device contains 65x132 bits of display data RAM and there is a one-to-one correspondence between the LCD panel pixels and the internal RAM bits.

The EM62100 chip can drive a 65x132 dot display, so that a single chip of EM62100 can drive a maximum of 65x132 or 55x132 or 49x132 or 33x132 dots display with the pad option (DUTY1, DUTY0). Moreover, the capacity of the display can be extended by master/slave structures between chips. The chips can minimize power consumption since no external operating clock is necessary for the RAM read/write operation. Furthermore, each chip has a built-in low-power LCD driver power supply, on-chip resistors for LCD driver power voltage adjustment and a built-in display clock CR oscillator circuit, hence, the EM62100 chip can be used to create the lowest power display system with the fewest components for high-performance portable devices.

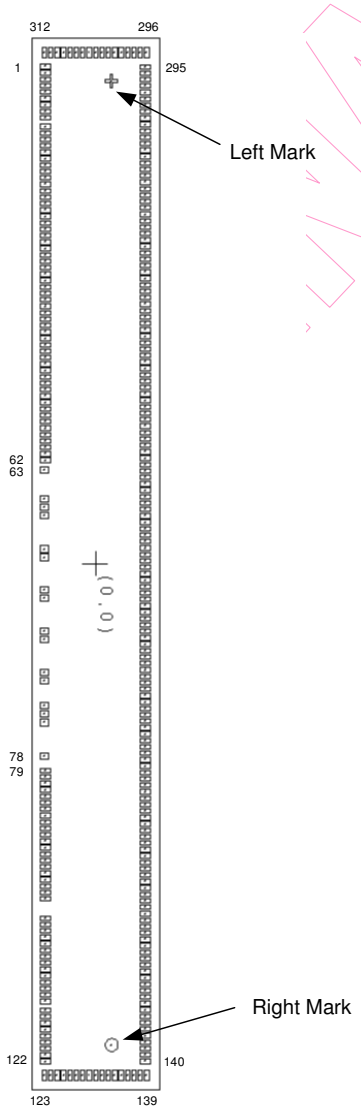
2 Features

- Direct display of RAM data through the display data RAM. RAM bit data: "0": non-illuminated "1": illuminated (at normal display)
- RAM capacity of 65*132 = 8,580 bits
- Display driver circuits: 65 common output and 132 segment outputs
- High-speed 8-bit MPU interface (80-series and 68-series) / Serial interfaces are supported.
- Multiple command functions: display data Read/Write, display ON/OFF, status read, Normal/Reverse display mode, page address set, display start line set, column address set, entire display ON/OFF, LCD bias set, electronic volume, read-modify-write, segment driver direction select, power saving, static indicator, common output status select, V0 voltage regulation internal resistor ratio set.
- Other command functions: Partial display, partial start line set, N-Line inversion.
- Built-in Static drive circuit for indicators
- Built-in low-power LCD power supply circuit: Booster circuit (with Boost ratios of two/three/four/five times, where the step-up voltage reference power supply can be input externally), High-accuracy voltage adjustment circuit (external input), built-in V0 voltage regulator resistors, built-in V1 to V4 voltage divider resistors, built-in electronic volume function, and voltage follower.

- Internal RC oscillator circuit (external clock can also be input)
- Extremely low power consumption
- Power supply, operable on the low 1.8 voltage,
  Logic power supply VDD – VSS = 1.8 to 3.6V,
  Boost reference voltage: VEE= 1.8 to 3.6V,
  LCD driver power supply: VLCD=V0 – VSS =4.0 to 14.2 V
- These chips are not designed with resistance to light or resistance to radiation.
- Package (Ordering information)

Part No.	Package Type
EM62100AGH	Gold Bump

3 Pin Configuration



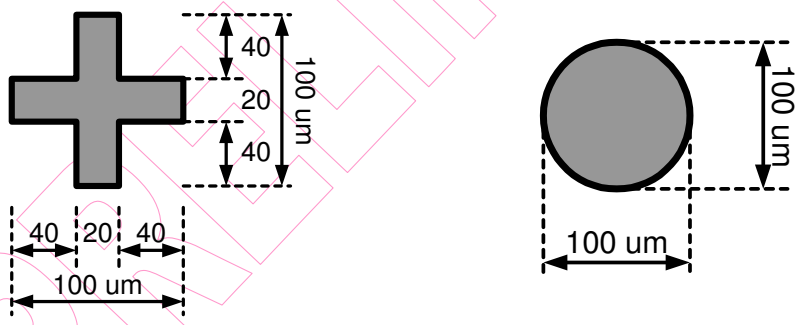
3.1 PIN DIMENSIONS

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	8200	1000	μm
Bump Size	1 ~ 62 , 79~122 , 140 ~ 295	35	80	
	123 ~ 139 , 296 ~ 312	80	35	
	63 ~78	50	58	
Pad Pitch	50 (min.)			
Die thickness (excluding bumps)	20 ±1 mil (525 ± 25μm)			
Bump Height	17 ± 2			
Minimum Bump Gap	15			
Coordinate Origin	Chip center			

3.2 MARK DIMENSIONS

Mark	Coordinate (X, Y)
Left	-3763.05 ,125.15
Right	3748.5 ,125.1

3.3 Alignment Key



3.4 Pin Coordinate Table

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y
1	NC1	-3877.5	-388.0	49	VEE	-1458.8	-388.0
2	COM57	-3827.5	-388.0	50	VEE	-1408.8	-388.0
3	COM58	-3777.5	-388.0	51	VEE	-1358.8	-388.0
4	COM59	-3727.5	-388.0	52	VEE	-1308.8	-388.0
5	COM60	-3677.5	-388.0	53	VEE	-1258.8	-388.0
6	COM61	-3627.5	-388.0	54	VSS	-1208.8	-388.0
7	COM62	-3577.5	-388.0	55	VSS	-1158.8	-388.0
8	COM63	-3527.5	-388.0	56	VSS	-1108.8	-388.0
9	COMS	-3477.5	-388.0	57	VSS	-1058.8	-388.0
10	NC2	-3408.8	-388.0	58	VSS	-1008.8	-388.0
11	FLM	-3358.8	-388.0	59	VSS	-958.8	-388.0
12	M	-3308.8	-388.0	60	VSS	-908.8	-388.0
13	CK	-325838	-388.0	61	VSS	-858.8	-388.0
14	DOFB	-3208.8	-388.0	62	TEST2	-808.8	-388.0
15	VSS	-3158.8	-388.0	63	VOUT	-733.65	-399.0
16	CS1B	-3108.8	-388.0	64	VOUT	-506.65	-399.0
17	CS2	-3058.8	-388.0	65	VOUT	-441.65	-399.0
18	VDD	-3008.8	-388.0	66	CAP4+	-376.65	-399.0
19	RESB	-2958.8	-388.0	67	CAP4+	-116.65	-399.0
20	RS	-2908.8	-388.0	68	CAP3+	-51.65	-399.0
21	WRB (RW)	-2858.8	-388.0	69	CAP3+	198.35	-399.0
22	TEST1	-2808.8	-388.0	70	CAP1-	263.35	-399.0
23	RDB (E)	-2758.8	-388.0	71	CAP1-	523.4	-399.0
24	VDD	-2708.8	-388.0	72	CAP1+	588.4	-399.0
25	D0	-2658.8	-388.0	73	CAP1+	845.4	-399.0
26	D0	-2608.8	-388.0	74	CAP2+	910.4	-399.0
27	D1	-2558.8	-388.0	75	CAP2+	1105.4	-399.0
28	D1	-2508.8	-388.0	76	CAP2+	1170.4	-399.0
29	D2	-2458.8	-388.0	77	CAP2-	1235.4	-399.0
30	D2	-2408.8	-388.0	78	CAP2-	1495.4	-399.0
31	D3	-2358.8	-388.0	79	V1	1610.1	-388.0
32	D3	-2308.8	-388.0	80	V1	1660.1	-388.0
33	D4	-2258.8	-388.0	81	V1	1710.1	-388.0
34	D4	-2208.8	-388.0	82	V1	1760.1	-388.0
35	D5	-2158.8	-388.0	83	V2	1810.1	-388.0
36	D5	-2108.8	-388.0	84	V2	1860.1	-388.0
37	D6	-2058.8	-388.0	85	V2	1910.1	-388.0
38	D6	-2008.8	-388.0	86	V2	1960.1	-388.0
39	D7	-1958.8	-388.0	87	V3	2010.1	-388.0
40	D7	-1908.8	-388.0	88	V3	2060.1	-388.0
41	DUTY0	-1858.8	-388.0	89	V3	2110.1	-388.0
42	VSS	-1808.8	-388.0	90	V3	2160.1	-388.0
43	DUTY1	-1758.8	-388.0	91	V4	2210.1	-388.0
44	VDD	-1708.8	-388.0	92	V4	2260.1	-388.0
45	VDD	-1658.8	-388.0	93	V4	2310.1	-388.0
46	VDD	-1608.8	-388.0	94	V4	2360.1	-388.0
47	VDD	-1558.8	-388.0	95	V0	2410.1	-388.0
48	VEE	-1508.8	-388.0	96	V0	2460.1	-388.0

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y
97	V0	2510.1	-388.0	145	COM4	3625.0	388.0
98	V0	2560.1	-388.0	146	COM3	3575.0	388.0
99	V0	2610.1	-388.0	147	COM2	3525.0	388.0
100	VREF	2758.8	-388.0	148	COM1	3475.0	388.0
101	TEST3	2808.8	-388.0	149	COM0	3425.0	388.0
102	VDD	2858.8	-388.0	150	COMS	3375.0	388.0
103	M/S	2908.8	-388.0	151	NC8	3325.0	388.0
104	CKS	2958.8	-388.0	152	SEG0	3275.0	388.0
105	VSS	3008.8	-388.0	153	SEG1	3225.0	388.0
106	M86	3058.8	-388.0	154	SEG2	3175.0	388.0
107	P/S	3108.8	-388.0	155	SEG3	3125.0	388.0
108	VDD	3158.8	-388.0	156	SEG4	3075.0	388.0
109	HPMB	3208.8	-388.0	157	SEG5	3025.0	388.0
110	VSS	3258.8	-388.0	158	SEG6	2975.0	388.0
111	IRS	3308.8	-388.0	159	SEG7	2925.0	388.0
112	VDD	3358.8	-388.0	160	SEG8	2875.0	388.0
113	NC3	3408.8	-388.0	161	SEG9	2825.0	388.0
114	COM31	3477.5	-388.0	162	SEG10	2775.0	388.0
115	COM30	3527.5	-388.0	163	SEG11	2725.0	388.0
116	COM29	3577.5	-388.0	164	SEG12	2675.0	388.0
117	COM28	3627.5	-388.0	165	SEG13	2625.0	388.0
118	COM27	3677.5	-388.0	166	SEG14	2575.0	388.0
119	COM26	3727.5	-388.0	167	SEG15	2525.0	388.0
120	COM25	3777.5	-388.0	168	SEG16	2475.0	388.0
121	COM24	3827.5	-388.0	169	SEG17	2425.0	388.0
122	NC4	3877.5	-388.0	170	SEG18	2375.0	388.0
123	NC5	3988.0	-400.0	171	SEG19	2325.0	388.0
124	COM23	3988.0	-350.0	172	SEG20	2275.0	388.0
125	COM22	3988.0	-300.0	173	SEG21	2225.0	388.0
126	COM21	3988.0	-250.0	174	SEG22	2175.0	388.0
127	COM20	3988.0	-200.0	175	SEG23	2125.0	388.0
128	COM19	3988.0	-150.0	176	SEG24	2075.0	388.0
129	COM18	3988.0	-100.0	177	SEG25	2025.0	388.0
130	COM17	3988.0	-50.0	178	SEG26	1975.0	388.0
131	COM16	3988.0	0.0	179	SEG27	1925.0	388.0
132	COM15	3988.0	50.0	180	SEG28	1875.0	388.0
133	COM14	3988.0	100.0	181	SEG29	1825.0	388.0
134	COM13	3988.0	150.0	182	SEG30	1775.0	388.0
135	COM12	3988.0	200.0	183	SEG31	1725.0	388.0
136	COM11	3988.0	250.0	184	SEG32	1675.0	388.0
137	COM10	3988.0	300.0	185	SEG33	1625.0	388.0
138	COM9	3988.0	350.0	186	SEG34	1575.0	388.0
139	NC6	3988.0	400.0	187	SEG35	1525.0	388.0
140	NC7	3875	388.0	188	SEG36	1475.0	388.0
141	COM8	3825	388.0	189	SEG37	1425.0	388.0
142	COM7	3775	388.0	190	SEG38	1375.0	388.0
143	COM6	3725	388.0	191	SEG39	1325.0	388.0
144	COM5	3675	388.0	192	SEG40	1275.0	388.0

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y
193	SEG41	1225.0	388.0	241	SEG89	-1175.0	388.0
194	SEG42	1175.0	388.0	242	SEG90	-1225.0	388.0
195	SEG43	1125.0	388.0	243	SEG91	-1275.0	388.0
196	SEG44	1075.0	388.0	244	SEG92	-1325.0	388.0
197	SEG45	1025.0	388.0	245	SEG93	-1375.0	388.0
198	SEG46	975.0	388.0	246	SEG94	-1425.0	388.0
199	SEG47	925.0	388.0	247	SEG95	-1475.0	388.0
200	SEG48	875.0	388.0	248	SEG96	-1525.0	388.0
201	SEG49	825.0	388.0	249	SEG97	-1575.0	388.0
202	SEG50	775.0	388.0	250	SEG98	-1625.0	388.0
203	SEG51	725.0	388.0	251	SEG99	-1675.0	388.0
204	SEG52	675.0	388.0	252	SEG100	-1725.0	388.0
205	SEG53	625.0	388.0	253	SEG101	-1775.0	388.0
206	SEG54	575.0	388.0	254	SEG102	-1825.0	388.0
207	SEG55	525.0	388.0	255	SEG103	-1875.0	388.0
208	SEG56	475.0	388.0	256	SEG104	-1925.0	388.0
209	SEG57	425.0	388.0	257	SEG105	-1975.0	388.0
210	SEG58	375.0	388.0	258	SEG106	-2025.0	388.0
211	SEG59	325.0	388.0	259	SEG107	-2075.0	388.0
212	SEG60	275.0	388.0	260	SEG108	-2125.0	388.0
213	SEG61	225.0	388.0	261	SEG109	-2175.0	388.0
214	SEG62	175.0	388.0	262	SEG110	-2225.0	388.0
215	SEG63	125.0	388.0	263	SEG111	-2275.0	388.0
216	SEG64	75.0	388.0	264	SEG112	-2325.0	388.0
217	SEG65	25.0	388.0	265	SEG113	-2375.0	388.0
218	SEG66	-25.0	388.0	266	SEG114	-2425.0	388.0
219	SEG67	-75.0	388.0	267	SEG115	-2475.0	388.0
220	SEG68	-125.0	388.0	268	SEG116	-2525.0	388.0
221	SEG69	-175.0	388.0	269	SEG117	-2575.0	388.0
222	SEG70	-225.0	388.0	270	SEG118	-2625.0	388.0
223	SEG71	-275.0	388.0	271	SEG119	-2675.0	388.0
224	SEG72	-325.0	388.0	272	SEG120	-2725.0	388.0
225	SEG73	-375.0	388.0	273	SEG121	-2775.0	388.0
226	SEG74	-425.0	388.0	274	SEG122	-2825.0	388.0
227	SEG75	-475.0	388.0	275	SEG123	-2875.0	388.0
228	SEG76	-525.0	388.0	276	SEG124	-2925.0	388.0
229	SEG77	-575.0	388.0	277	SEG125	-2975.0	388.0
230	SEG78	-625.0	388.0	278	SEG126	-3025.0	388.0
231	SEG79	-675.0	388.0	279	SEG127	-3075.0	388.0
232	SEG80	-725.0	388.0	280	SEG128	-3125.0	388.0
233	SEG81	-775.0	388.0	281	SEG129	-3175.0	388.0
234	SEG82	-825.0	388.0	282	SEG130	-3225.0	388.0
235	SEG83	-875.0	388.0	283	SEG131	-3275.0	388.0
236	SEG84	-925.0	388.0	284	NC9	-3325.0	388.0
237	SEG85	-975.0	388.0	285	COM32	-3375.0	388.0
238	SEG86	-1025.0	388.0	286	COM33	-3425.0	388.0
239	SEG87	-1075.0	388.0	287	COM34	-3475.0	388.0
240	SEG88	-1125.0	388.0	288	COM35	-3525.0	388.0

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y
289	COM36	-3575.0	388.0	301	COM46	-3988.0	150.0
290	COM37	-3625.0	388.0	302	COM47	-3988.0	100.0
291	COM38	-3675.0	388.0	303	COM48	-3988.0	50.0
292	COM39	-3725.0	388.0	304	COM49	-3988.0	0.0
293	COM40	-3775.0	388.0	305	COM50	-3988.0	-50.0
294	COM41	-3825.0	388.0	306	COM51	-3988.0	-100.0
295	NC10	-3875.0	388.0	307	COM52	-3988.0	-150.0
296	NC11	-3988.0	400.0	308	COM53	-3988.0	-200.0
297	COM42	-3988.0	350.0	309	COM54	-3988.0	-250.0
298	COM43	-3988.0	300.0	310	COM55	-3988.0	-300.0
299	COM44	-3988.0	250.0	311	COM56	-3988.0	-350.0
300	COM45	-3988.0	200.0	312	NC12	-3988.0	-400.0

4 Pin Description

Table 1

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>VDD</td><td>Power Supply</td><td>Power supply terminal VCC</td><td>8</td></tr>
<tr><td>VSS</td><td>Power Supply</td><td>System Ground</td><td>12</td></tr>
<tr><td>VEE</td><td>Power Supply</td><td>Voltage supply pin for booster circuit. Usually the same voltage level as VDD.</td><td>6</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>Power Supply</td><td>Multi-level power supply for the liquid crystal drive. The voltage applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divider or by changing the impedance using an Op. Amp. Voltage levels are determined based on V_0, and must maintain the relative magnitudes shown below.
V0≥V1≥V2≥V3≥V4≥VSS
Master operation: When the power supply is turned ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.
<table>
<tr><th>LCD bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/4 bias</td><td>3/4V0</td><td>2/4V0</td><td>2/4V0</td><td>1/4V0</td></tr>
<tr><td>1/5 bias</td><td>4/5V0</td><td>3/5V0</td><td>2/5V0</td><td>1/5V0</td></tr>
<tr><td>1/6 bias</td><td>5/6V0</td><td>4/6V0</td><td>2/6V0</td><td>1/6V0</td></tr>
<tr><td>1/7 bias</td><td>6/7V0</td><td>5/7V0</td><td>2/7V0</td><td>1/7V0</td></tr>
<tr><td>1/8 bias</td><td>7/8V0</td><td>6/8V0</td><td>2/8V0</td><td>1/8V0</td></tr>
<tr><td>1/9 bias</td><td>8/9V0</td><td>7/9V0</td><td>2/9V0</td><td>1/9V0</td></tr>
</table></td><td>21</td></tr>
<tr><td>CAP1+</td><td>O</td><td>Capacitor 1 positive pin for voltage converter</td><td>2</td></tr>
<tr><td>CAP1-</td><td>O</td><td>Capacitor 1 negative pin for voltage converter</td><td>2</td></tr>
<tr><td>CAP2+</td><td>O</td><td>Capacitor 2 positive pin for voltage converter</td><td>2</td></tr>
<tr><td>CAP2-</td><td>O</td><td>Capacitor 2 negative pin for voltage converter</td><td>3</td></tr>
<tr><td>CAP3+</td><td>O</td><td>Capacitor 3 positive pin for voltage converter</td><td>2</td></tr>
<tr><td>CAP4+</td><td>O</td><td>Capacitor 4 positive pin for voltage converter</td><td>2</td></tr>
<tr><td>VOUT</td><td>I/O</td><td>DC/DC voltage converter input/output pin, connect a capacitor between this terminal and VSS</td><td>3</td></tr>
<tr><td>VREF</td><td>I</td><td>V0 voltage adjustment pad. Applies voltage between V0 and VSS using a resistive divider. This is only enabled (IRS=“L”) When the V0 voltage regulator internal resistor is not used. When the V0 voltage regulator internal resistor is used (IRS=“H”), this pin must be floating.</td><td>1</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>DUTY0
DUTY1</td><td>I</td><td>Select the maximum LCD driver duty
<table>
<tr><th>DUTY1</th><th>DUTY 0</th><th>LCD Driver Duty</th></tr>
<tr><td>0</td><td>0</td><td>1/33</td></tr>
<tr><td>0</td><td>1</td><td>1/49</td></tr>
<tr><td>1</td><td>0</td><td>1/55</td></tr>
<tr><td>1</td><td>1</td><td>1/65</td></tr>
</table></td><td>2</td></tr>
<tr><td>D0, D1,
D2, D3,
D4, D5,
D6 (SCL),
D7 (SI)</td><td>I/O</td><td>8-bit bi-directional data bus connected to an 8-bit or 16-bit standard MPU data bus. When the chip select is inactive, D0 to D7 are set to high impedance.
When serial interface is selected (P/S = “L”), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). During this time, D0 to D5 are set to high impedance.</td><td>16</td></tr>
<tr><td>RS</td><td>I</td><td>Determines whether the data bits are data or instruction (command).
<table>
<tr><th>RS</th><th>D0 to D7</th></tr>
<tr><td>H</td><td>Display data</td></tr>
<tr><td>L</td><td>Instruction (Command)</td></tr>
</table></td><td>1</td></tr>
<tr><td>RESB</td><td>I</td><td>When RESB is set to “L,” the settings are initialized.</td><td>19</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select signal. When CS1B = “L” and CS2 = “H,” then the chip select CS2 becomes active, and data/command I/O is enabled.</td><td>2</td></tr>
<tr><td>RDB (E)</td><td>I</td><td>Enable clock signal input for the 68-series MPU, active high.
Active low input pin for the 80-series MPU RDB signal</td><td>1</td></tr>
<tr><td>WRB (RW)</td><td>I</td><td>Read/Write control signal with 68-series MPU
RW=”H”: Read, RW=”L”: Write
Active low input pin for the 80 series MPU WRB signal</td><td>1</td></tr>
<tr><td>M86</td><td>I</td><td>MPU interface switch terminal
M86 =”H”: 68-series MPU interface
M86 =”L”: 80-series MPU interface</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Selects the Parallel or Serial data input interface
P/S = “H”: Parallel data input interface, P/S = “L”: Serial data input interface
The following applies depending on the P/S status:
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>H</td><td>RS</td><td>D0 to D7</td><td>RDB (E),
WRB (RW)</td><td></td></tr>
<tr><td>L</td><td>RS</td><td>D7 (SI)</td><td>Write only</td><td>D6 (SCL)</td></tr>
</table>
When P/S = “L”, D0 to D5 are hi-Z. D0 to D5 can be “H” or “L”
RDB (E) and WRB (RW) are fixed to either “H” or “L”. With serial data input, RAM display data reading is not supported.</td><td>1</td></tr>
<tr><td>CKS</td><td>I</td><td>Terminal to select whether enable or disable the display clock internal oscillator circuit.
CKS = “H”: Internal oscillator circuit is enabled
CKS = “L”: Internal oscillator circuit is disabled
(requires an external input)
When CKS = “L”, input the display clock through the CK terminal.</td><td>1</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>M/S</td><td>I</td><td>M/S = “H”: Master operation
M/S = “L”: Slave operation
The following is true depending on the M/S and CKS status:
<table>
<tr><th>M/S</th><th>CKS</th><th>Oscillator Circuit</th><th>Power Supply Circuit</th><th>CK</th><th>M</th><th>FLM</th><th>DOFB</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Enable</td><td>Enable</td><td>O</td><td>O</td><td>O</td><td>O</td></tr>
<tr><td>L</td><td>Disable</td><td>Enable</td><td>I</td><td>O</td><td>O</td><td>O</td></tr>
<tr><td>L</td><td>-</td><td>Disable</td><td>Disable</td><td>I</td><td>I</td><td>O</td><td>I</td></tr>
</table>
O: Output, I: Input</td><td>1</td></tr>
<tr><td>CK</td><td>I/O</td><td>Display clock input terminal
When the EM62100 chips are used in master/slave mode, the various CK terminals must be connected.</td><td>1</td></tr>
<tr><td>M</td><td>I/O</td><td>Liquid crystal alternating current signal I/O terminal.
M/S = “H”: Output, M/S = “L”: Input
When the EM62100 Series chip is used in master/slave mode, the various M terminals must be connected.</td><td>1</td></tr>
<tr><td>DOFB</td><td>I/O</td><td>LCD blanking control terminal
M/S = “H”: Output, M/S = “L”: Input
When the EM62100 chip is used in master/slave mode, the various DOFB terminals must be connected.</td><td>1</td></tr>
<tr><td>FLM</td><td>O</td><td>Output terminal for the static drive
This terminal is only enabled when the static indicator display is ON during master mode operation, and is used in connection with the M terminal.</td><td>1</td></tr>
<tr><td>IRS</td><td>I</td><td>This terminal selects the resistors for the V0 voltage level adjustment.
IRS = “H”: Use the internal resistors
IRS = “L”: Do not use the internal resistors. The V0 voltage level is regulated by an external resistive voltage divider attached to the VREF terminal.
This pin is enabled only when master mode operation is selected. It is fixed to either “H” or “L” when slave mode operation is selected.</td><td>1</td></tr>
<tr><td>HPMB</td><td>I</td><td>Power control terminal for the power supply circuit for liquid crystal drive.
HPMB = “H”: Normal mode, HPMB = “L”: High power mode
This pin is enabled only when master mode operation is selected. It is fixed to either “H” or “L” when slave mode operation is selected.</td><td>1</td></tr>
<tr><td>SEG0
To
SEG131</td><td>O</td><td>Liquid crystal segment drive outputs. Through a combination of the contents of the display RAM and with the M signal, a single level is selected from V0, V2, V3, and VSS.
<table>
<tr><th colspan="2">RAM DATA</th><th>M</th><th colspan="2">Output Voltage</th></tr>
<tr><td colspan="2"></td><td></td><td>Normal Display</td><td>Reverse Display</td></tr>
<tr><td colspan="2">H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td colspan="2">H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td colspan="2">L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td colspan="2">L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Power Save & Display OFF</td><td>--</td><td colspan="2">VSS</td></tr>
</table></td><td>132</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>COM0
To
COM63</td><td>O</td><td>LCD common drive outputs.
Through a combination of the contents of the scan data and with the M signal, a single level is selected from V0, V1, V4, and VSS.

<table><tr><th>Scan Data</th><th>M</th><th>Output Voltage</th></tr><tr><td>H</td><td>H</td><td>VSS</td></tr><tr><td>H</td><td>L</td><td>V0</td></tr><tr><td>L</td><td>H</td><td>V1</td></tr><tr><td>L</td><td>L</td><td>V4</td></tr><tr><td>Power Save</td><td>--</td><td>VSS</td></tr></table></td><td>64</td></tr>
<tr><td>COMS</td><td>O</td><td>Common output terminals for the indicator. Both terminals output the same signal. Leave these open if they are not used.
When in master/slave mode, the same signal is output by both master and slave.</td><td>2</td></tr>
<tr><td>TEST1~3</td><td>I/O</td><td>For IC chip testing. Must be floating.</td><td>3</td></tr>
</table>

5 Block Diagram

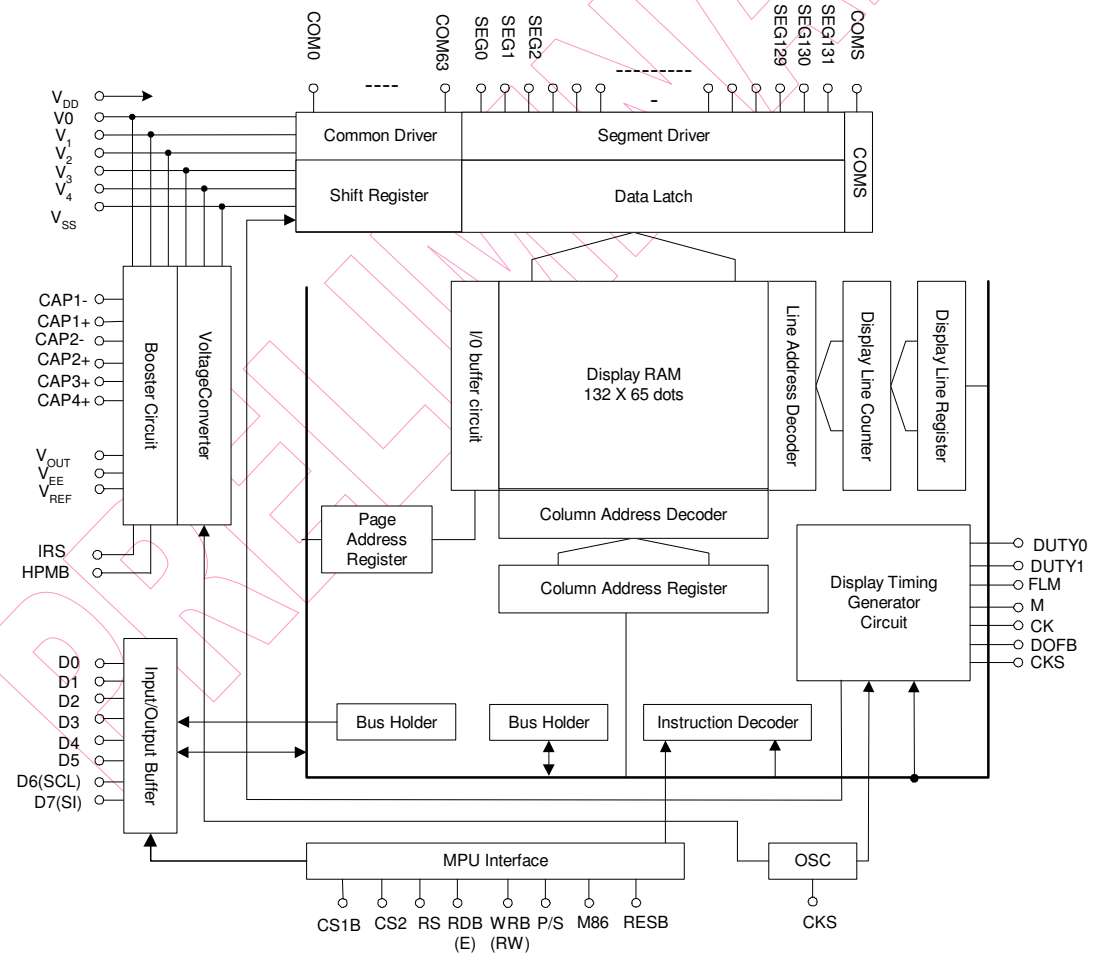


Fig. 1 System Block Diagram

6 Function Description

6.1 MPU Interface

6.1.1 Selecting the Interface Type

The EM62100 chip has three types of interface with an MPU, which are two parallel interfaces and serial interface. The interface is determined by the P/S terminal polarity to the “H” or “L”, as shown in Table 2.

Table 2

P/S	CS1B	CS2	RS	RDB	WRB	M86	D7	D6	D5~D0
H: Parallel Input	CS1B	CS2	RS	RDB	WRB	M86	D7	D6	D5~D0
L: Serial Input	CS1B	CS2	RS	--	--	--	SI	SCL	(Hi-Z)

“--“Indicates fixed to either “H” or to “L”

6.1.2 Parallel Interface

When the parallel interface has been selected (P/S=”H”), then it is possible to connect directly to either an 8080-series MPU or a 6800-series MPU by selecting the M86 terminal to either “H” or to “L”.

Table 3

M86	CS1B	CS2	RS	RDB	WRB	D7~D0
L: 80-series MPU	CS1B	CS2	RS	RDB	WRB	D7~D0
H: 68-series MPU	CS1B	CS2	RS	E	RW	D7~D0

The type of data transfer is determined by signals at RS, RDB (E), WRB (RW) as shown in Table 4.

Table 4

RS	68-Series	80-Series		Function
	RW	RDB	WRB	
1	1	0	1	Reads display data
1	0	1	0	Writes display data
0	1	0	1	Read status
0	0	1	0	Write control data (command)

6.1.3 Serial Interface

When the EM62100 is active (CS1B="L" and CS2="H"), the serial data input (SI) and the serial clock input (SCL) can be received. The serial data can be read from the SI pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the 8th serial clock for processing.

The RS input is used to determine whether the serial data input is display data (RS="H") or command data (RS="L"). The RS input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active. Figure 2 is a serial interface signal chart.

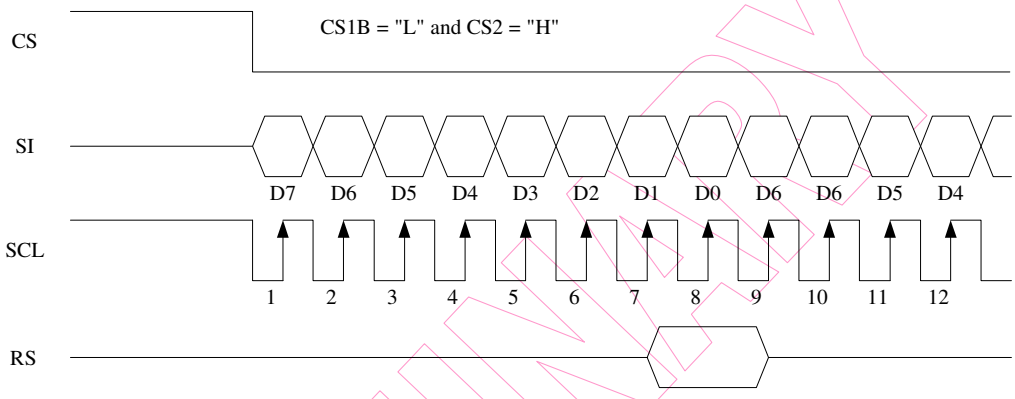


Fig. 2

NOTE

1. *When the chip is not active, the shift registers and counter are reset to their initial states.*
2. *Reading is not possible while in serial interface mode.*
3. *Caution is required on the SCL signal when it comes to line-end reflections and external noise. It is recommended that operation be rechecked on the actual equipment.*

6.1.4 Chip Select

The EM62100 has two chip select terminals: CS1B and CS2. The MPU interface or the serial interface is enabled only when CS1B="L" and CS2="H". When the chip select is non-active D0 to D7 enter high impedance and the RS, RDB, and WRB inputs are inactive. When the serial interface is selected, the shift register and the counter are reset.

6.2 Access to Display Data RAM and Internal Registers

To match operation frequencies between the MPU and display RAM or internal register, the EM62100 performs an LSI-LSI pipelining via the bus holder attached to the internal data bus.

When the MPU writes data to the display RAM, once the data is stored in the bus holder, then it is written to the display RAM before the next data write cycle. Moreover, when the MPU reads the display RAM, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle.

There is a certain restriction in the read sequence of the display RAM. It should be noted that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated during the second time data read. Thus, a dummy read is required whenever the address setup or the write cycle operation is performed. This relationship is shown in Figure 3.

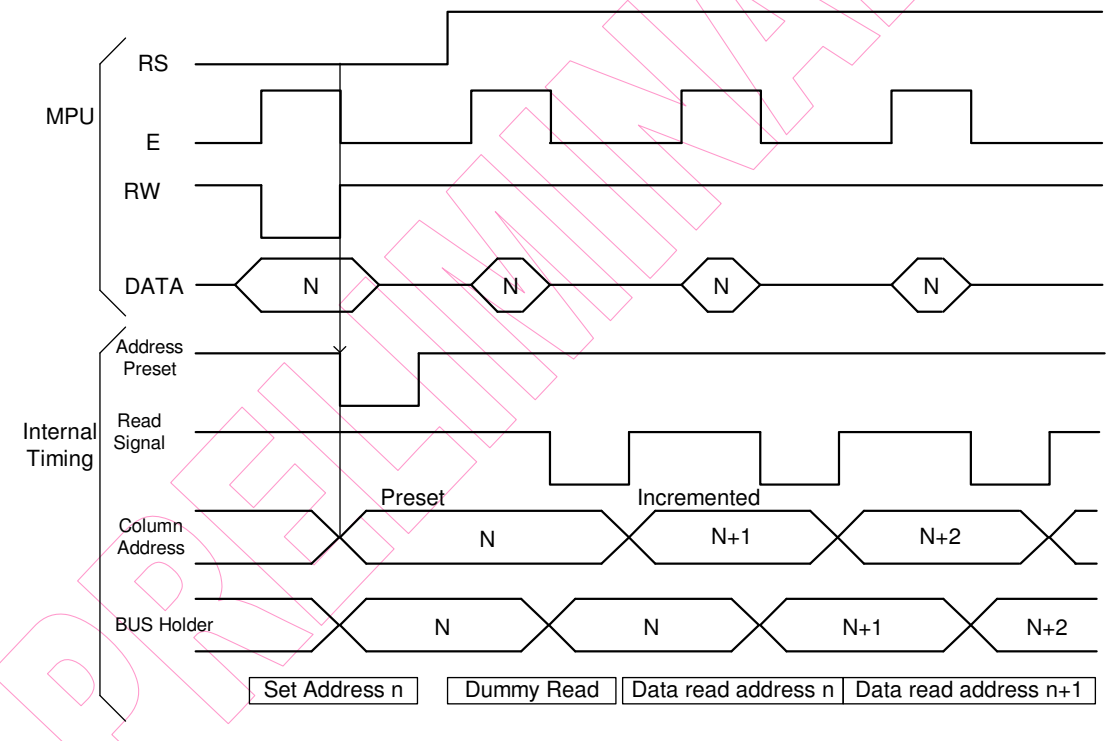


Fig. 3

6.3 Busy Flag

The busy flag is output to pin D7 by a read status command. When the busy flag is "1" it indicates that the EM62100 chip is executing its internal operations, any command other than status read is ignored during this time. If the cycle time (t_{CYC}) is correct, this flag need not be checked before each instruction. This makes vast improvements in MPU processing capabilities possible.

6.4 Display Data RAM

The display data RAM stores the pixel data for the LCD. It is a 65×132 addressable array. It allows access to the desired bit by specifying the page address and the column address. The 65 rows are divided into 8 pages of 8 lines and the 9th page with a single line (D0). The D7 to D0 display data from the MPU corresponds to the LCD common lines as show in *Fig.4*. There are few constraints at the time of display data transfer when multiple EM62100 chip is used. However, the display structures can be created easily and with a high degree of freedom. Reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously, it will not cause adverse effects on the display (such as flickering).

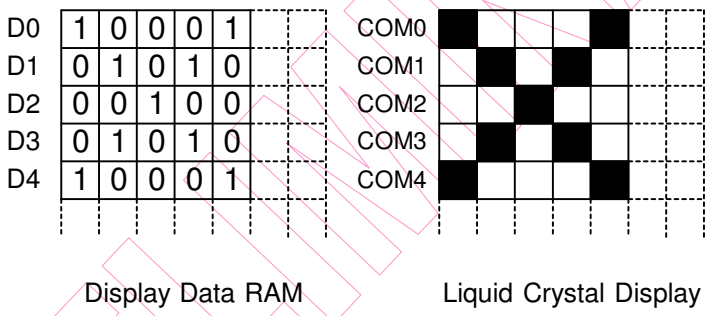


Fig. 4

6.5 Page Address Circuit

The page address of the display data RAM is specified through the Page Address Set Command. The page address needs to be specified again in accessing other pages. Page address 8 is the page for the RAM region used only by the static indicators, and only display data D0 is used.

6.6 Line Address Circuit

The line address circuit assigns the line address corresponding to the common output when the contents of the display data RAM are displayed. Using the display start line address set command, the normal top line of the display can be specified (which is the COM0 output when the common output mode is normal, and the COM63 output for EM62100 when the common output mode is reversed. The display area is a 65-line area for the EM62100 from the display start line address.

If the line address is changed dynamically using the display start line address set command, screen scrolling, page swapping, etc., can be performed.

6.7 Column Addresses Circuit

The column address is specified by the Column Address Set command, as shown in Fig.5. The specified column address is incremented by 1 each time a read or write display data instruction is executed. This allows the MPU display data to be accessed continuously. The column address can no longer be incremented at 83H. Since the column address is independent of the page address, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to specify both the page address and the column address.

Furthermore, as shown in Table 4, the ADC command can be used to invert the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized.

Table 5

SEG Output	SEG0		SEG131
ADC"0"	0(H) →	Column address	→ 83(H)
ADC"1"	83(H) ←	Column address	← 0(H)

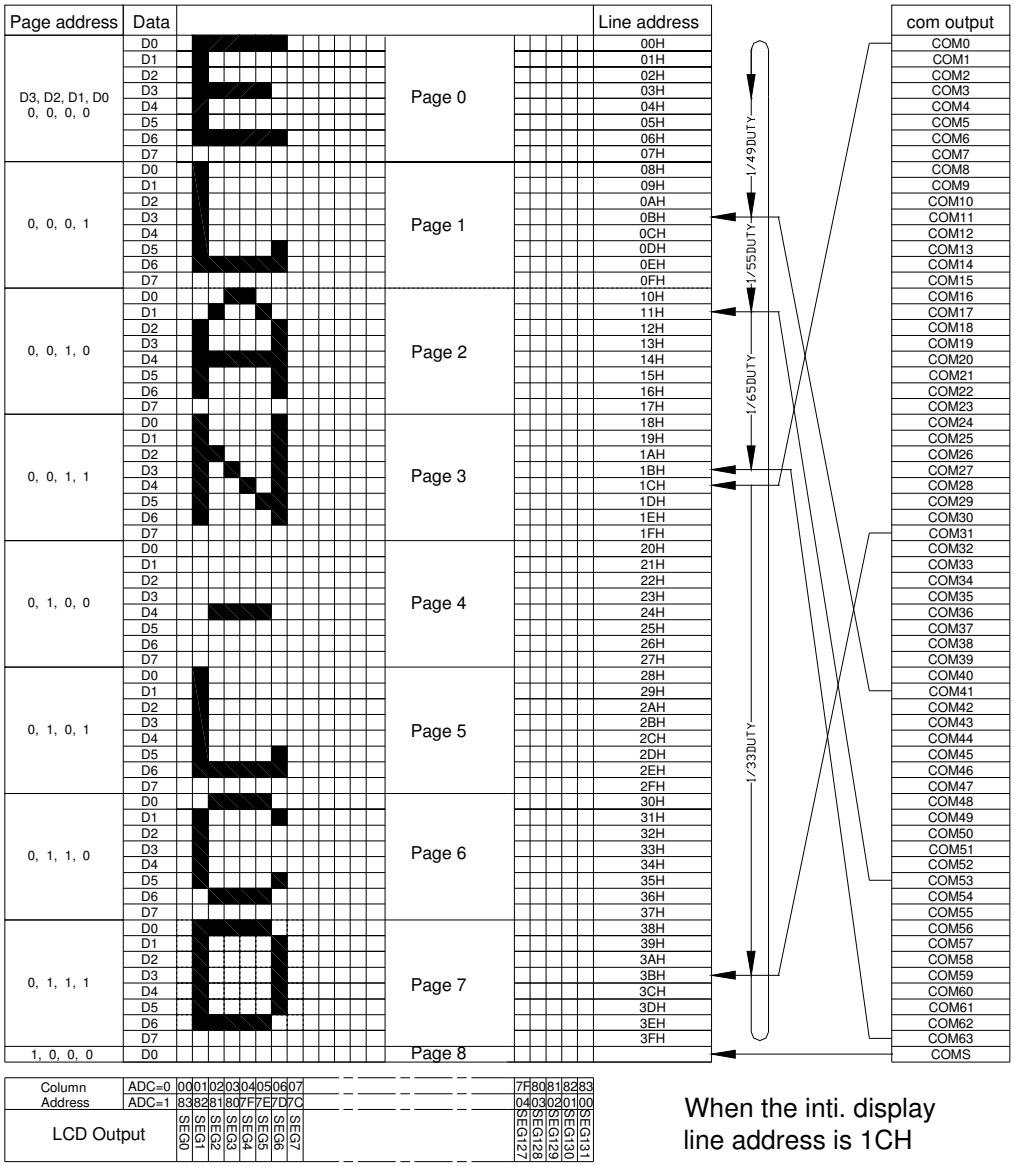


Fig. 5 Display Data RAM

6.8 Display Data Latch Circuit

The display data latch circuit temporarily stores the display data that is output to the LCD from the display data RAM. The commands such as display normal/reverse status, display ON/OFF status, and entire display ON/OFF, control only the data within the latch, but do not change the data within the display data RAM itself.

6.9 Oscillator Circuit

This is an RC type oscillator that generates the display clock. The oscillator circuit is only enabled when M/S="H" and CKS="H". When CKS="L" the oscillation stops, and the display clock is input through the CK terminal.

6.10 Display Timing Generator Circuit

This circuit generates some signals used for displaying the LCD. The display clock, CK generated by an oscillation clock, generates a clock to the line counter and a latch signal to the display data latch. The line address of the on-chip RAM is generated in synchronization with the display clock (CK) and the display data latch circuit in synchronization, latches the 132-bit display data with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor.

Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (M) from the display clock. It generates a drive waveform using a 2-frame alternating current drive method, as shown in Figure 6, for the liquid crystal drive circuit.

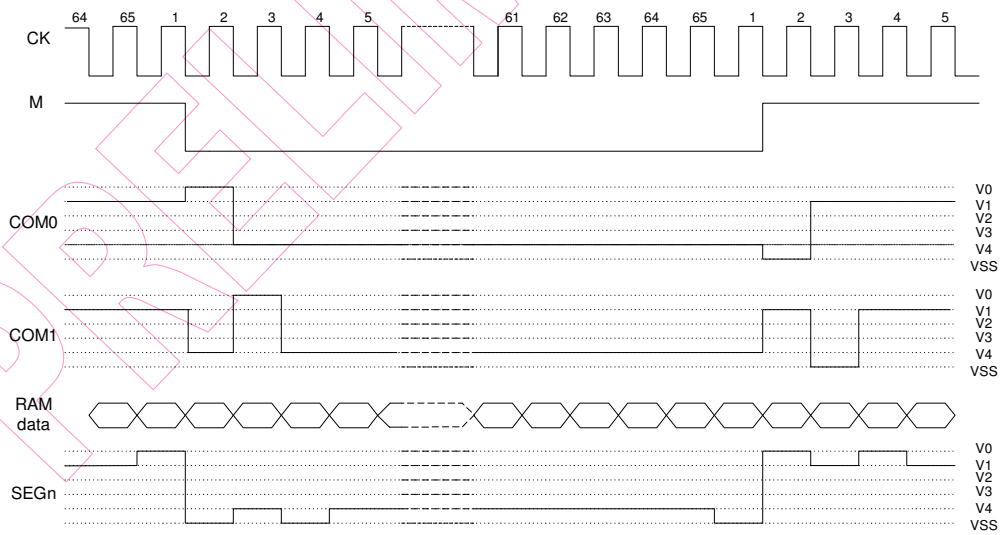


Figure 6

When several EM62100 chips are used, the slave chips must supply the display timing signals (M, CK, DOFB) from the master chip. Explanation is shown in Table 6.

Table 6

Operating Mode		M	CK	DOFB
Master (M/S= "H")	The internal oscillator circuit is enabled (CKS="H") The internal oscillator circuit is disabled (CKS="L")	O O	O I	O O
Slave (M/S = "L")	The internal oscillator circuit is enabled (CKS="H") The internal oscillator circuit is disabled (CKS="L")	I I	I I	I I

O: Output, I: Input

NOTE

When the EM62100 is used in the master/slave configuration, each of the CKS pins are set to the same level together.

Table 7 shows the relationship between the oscillation frequency and frame frequency. fOSC which can be selected as 31.4 or 26.3kHz by using Oscillation Frequency Select command.

Table 7

Duty	Item	fCK	fM
1/65	On-chip oscillator is used	fOSC/6	fCK / (2 x 65)
	On-chip oscillator is not used	External input fCL	fCK / (2 x 65)
1/55	On-chip oscillator is used	fOSC/7	fCK / (2 x 55)
	On-chip oscillator is not used	External input fCL	fCK / (2 x 55)
1/49	On-chip oscillator is used	fOSC/8	fCK / (2 x 49)
	On-chip oscillator is not used	External input fCL	fCK / (2 x 49)
1/33	On-chip oscillator is used	fOSC/12	fCK / (2 x 33)
	On-chip oscillator is not used	External input fCL	fCK / (2 x 33)
1/17	On-chip oscillator is used	fOSC/22	fCK / (2 x 17)
	On-chip oscillator is not used	External input fCL	fCK / (2 x 17)
1/9	On-chip oscillator is used	fOSC/44	fCK / (2 x 9)
	On-chip oscillator is not used	External input fCL	fCK / (2 x 9)

6.11 Common Control (Shift Register)

6.11.1 Common Number

This circuit controls the relationship between the number of common output and specified duty ratio. Common output mode select instruction specifies the scanning direction of the common output pads, as shown in Table 8.

Table 8

Duty	Status	Common Output Pads							
		COM [0:15]	COM [16:23]	COM [24:26]	COM [27:36]	COM [37:39]	COM [40:47]	COM [48:63]	COMS
1/33	Normal	COM[0:15]	NC					COM[16:31]	COMS
	Reverse	COM[31:16]	NC					COM[15:0]	COMS
1/49	Normal	COM[0:23]		NC			COM[24:47]		COMS
	Reverse	COM[47:24]		NC			COM[23:0]		COMS
1/55	Normal	COM[0:26]			NC		COM[27:53]		COMS
	Reverse	COM[53:27]			NC		COM[26:0]		COMS
1/65	Normal	COM[0:63]							COMS
	Reverse	COM[63:0]							COMS

6.11.2 LCD Driver Circuits

There are 197 channel drivers that generate four voltage levels for driving the liquid crystal. The combination of the display data, the COM scan signal, and the M signal produces the liquid crystal drive voltage output. Figure 7 shows examples of the SEG and COM output waveform.

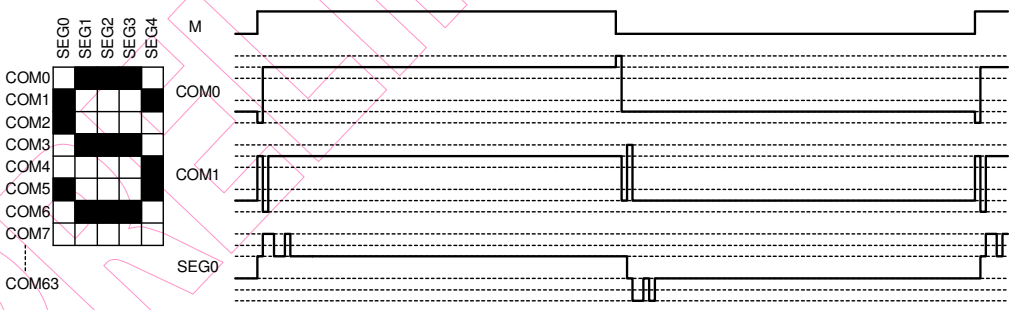


Fig. 7

6.11.3 Configuration Setting

The EM62100 has two-optional configurations, configured by DUTY0 and DUTY1, as shown in Table 9.

Table 9

Duty ratio	Duty1	Duty0	LCD bias	V1	V2	V3	V4
1/33	0	0	1/5	(4/5)V0	(3/5)V0	(2/5)V0	(1/5)V0
			1/6	(5/6)V0	(4/6)V0	(2/6)V0	(1/6)V0
1/49	0	1	1/6	(5/6)V0	(4/6)V0	(2/6)V0	(1/6)V0
			1/8	(7/8)V0	(6/8)V0	(2/8)V0	(1/8)V0
1/55	1	0	1/6	(5/6)V0	(4/6)V0	(2/6)V0	(1/6)V0
			1/8	(7/8)V0	(6/8)V0	(2/8)V0	(1/8)V0
1/65	1	1	1/7	(6/7)V0	(5/7)V0	(2/7)V0	(1/7)V0
			1/9	(8/9)V0	(7/9)V0	(2/9)V0	(1/9)V0

6.12 Power Supply Module

The power supply circuits have low power consumption and generate the voltage levels necessary to drive the LCD. There are Booster (step-up voltage) circuits, Voltage regulator circuits, and voltage follower circuits. They are valid only when operating in master mode.

The power supply circuit can turn the Booster circuits, the voltage regulator circuits and the voltage follower circuit ON or OFF independently through the Power Control Set command. Consequently, it is possible to make both external and internal power supplies function in parallel. Table 10 shows the Power Control Set Command 3-bit data control function. Table 11 shows the reference combinations.

Table 10

Item	Status	
	H	L
D2 Voltage Booster (V/B) circuit control bit	ON	OFF
D1 Voltage Regulator (V/R) circuit control bit	ON	OFF
D0 Voltage Follower (V/F) circuit control bit	ON	OFF

Table 11. Recommended Power Supply Combinations

Use Step-up	V/B	V/R	V/F	V/B Circuit	V/R Circuit	V/F Circuit	External Voltage Input	Step-up Voltage System Terminal
Only the internal power supply is used	1	1	1	ON	ON	ON	VEE	Used
Only the V/R circuit and V/F circuits are used	0	1	1	OFF	ON	ON	VOUT, VEE	Open
Only the V/F circuit is used	0	0	1	OFF	OFF	ON	V0, VEE	Open
Only the external power supply is used	0	0	0	OFF	OFF	OFF	V0 to V4	Open

NOTE

- *For the "Step-up system terminals" refer to CAP1+, CAP1-, CAP2+, CAP2-, CAP3+ and CAP4+.*
- *Other combinations, not shown above, are also possible, but such combinations are not recommended for they have no practical use.*

6.12.1 Step-up Voltage Circuit

With the built-in boost up voltage circuit of the EM62100 chip, it is possible to produce a 5X, 4X, 3X, and 2X step-up of the VEE voltage levels. The step-up voltage relationships are shown in Figure 8.

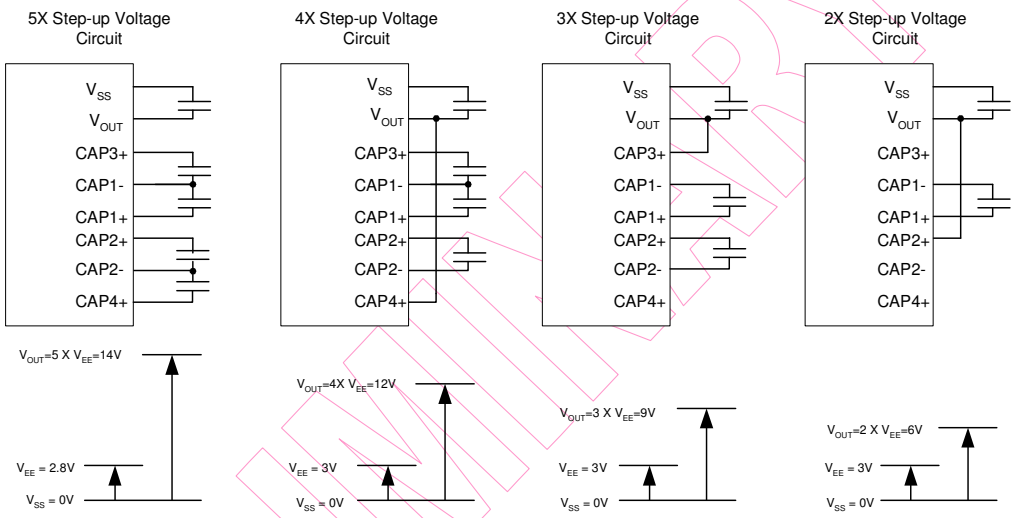


Fig. 8

6.12.2 Voltage Regulator Circuit

The step-up voltage generated at VOUT outputs the LCD driver voltage V0 through the voltage regulator circuit by adjusting resistors, Ra and Rb.

Because the EM62100 chip has an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.

- Using V0 voltage regulator internal resistors

  By using the V0 voltage regulator internal resistors and the electronic volume function, the liquid crystal power supply voltage V0 can be controlled through command executions alone (without adding external resistors), allowing for adjustments on the *LCD* brightness. The V0 voltage can be calculated using equation (a) over the range where V0<VOUT.

$$V0 = (1+\frac{Rb}{Ra}) \times VEV = (1+\frac{Rb}{Ra}) \times (1-\frac{63-\alpha}{162}) \times VREG \quad \text{---------- (a)}$$

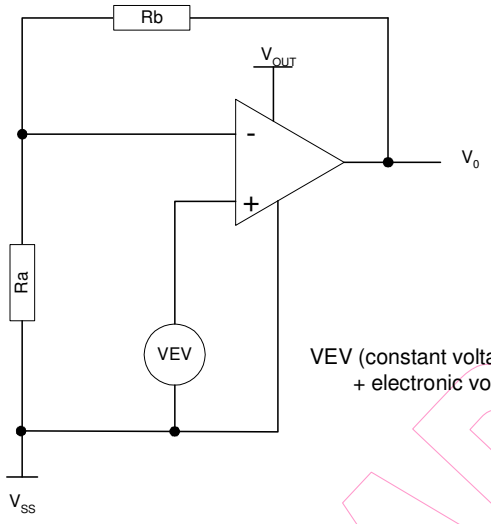


Fig. 9

VREG is the IC internal fixed voltage supply, and its voltage at Ta = 25℃ is as shown below.

Equipment Type	Thermal Gradient	Units	VREG
Internal power supply	-0.05	% / ℃	2.1

The α is set to 1 level of 64 possible levels of the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 12 shows the value for α depending on the electronic volume register settings.

Table 12

D5	D4	D3	D2	D1	D0	α	V0
0	0	0	0	0	0	0	Minimum
0	0	0	0	0	1	1	:
0	0	0	0	1	0	2	:
		:			:	:	:
1	0	0	0	0	0	32	(Default)
		:			:	:	:
1	1	1	1	1	0	62	:
1	1	1	1	1	1	63	Maximum

Rb/Ra is the V0 voltage regulator internal resistor ratio and can be set to 8 different levels through the V0 voltage regulator internal resistor ratio set command. The (1+Rb/Ra) ratio assumes the values shown in Table 13 depending on the 3-bit data settings in the V0 voltage regulator internal resistor ratio register.

Table 13

Register			Equipment Type by Thermal Gradient (Unit: % / ℃)
D2	D1	D0	-0.05
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0 (Default)
1	0	1	5.5
1	1	0	6.0
1	1	1	6.4

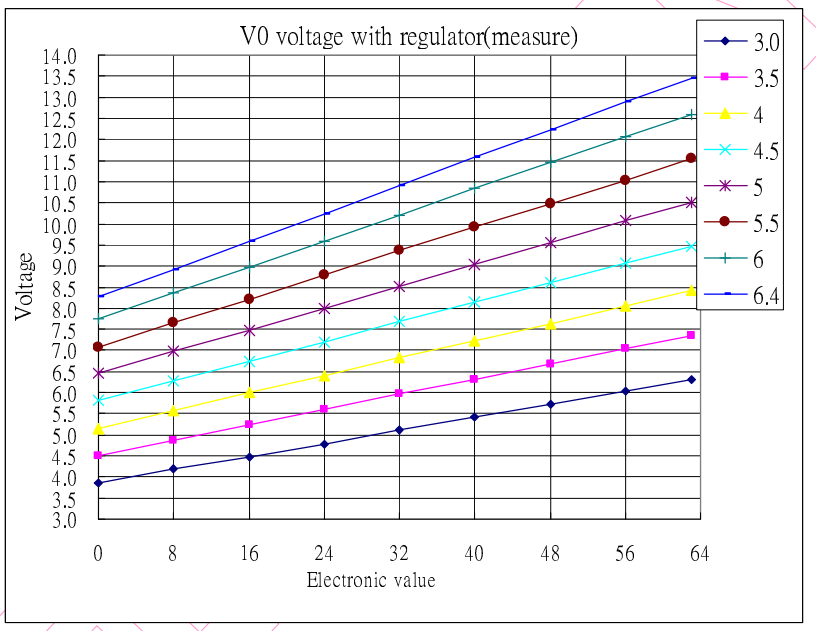


Fig.10 Contrast Curve of V_0 Voltage with Internal Resistors

6.12.3 Liquid Crystal Voltage Generator Circuit

The V0 voltage is produced by a resistive voltage divider within the IC, and can generate the V1, V2, V3, and V4 voltage levels required for LCD driving. Moreover, when the voltage follower changes the impedance, it provides V1, V2, V3, and V4 to the liquid crystal drive circuit. 1/9 bias or 1/7 bias for EM62100 can be selected.

6.12.4 High Power Mode

The EM62100 built-in power supply circuit has very low power consumption (normal mode: HPMB="H"). If used for LCD panels with large loads, this low-power power supply may cause the display quality to degrade. When this occurs, setting the HPMB terminal to "L" (high power mode) can improve the display quality. It is recommended that the display be checked on the actual equipment to determine whether or not to use this mode.

Moreover, if the improvement to the display is inadequate even after the high power mode has been set, then it is a must to add a Command Sequence when the Built-in Power Supply is turned OFF. To turn off the built-in power supply, follow the command sequence as shown below, wherein you have to turn it off after making the system enter the standby mode.

6.12.5 Reference Power Supply Circuit for Driving the LCD Panel

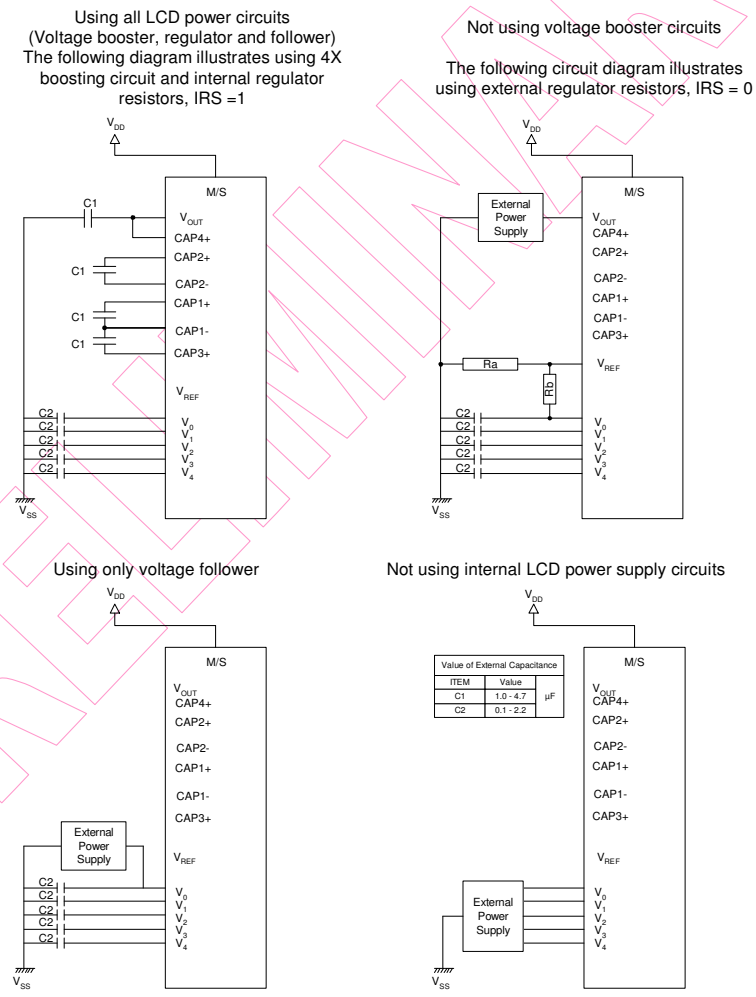


Fig.11

6.13 Reset Circuit

6.13.1 Initial Value of the Command Register

When the RESB input falls to “L”, the EM62100 will re-enter into its default state and the following conditions occur.

1. Display OFF
2. Normal display
3. ADC select: Normal display (ADC command D0 = “L”)
4. Power control register (D2, D1, D0) = (0, 0, 0,)
5. The serial interface register data is reset to its initial value.
6. LCD power supply bias ratio: 1/9 (1/65 duty), 1/8 (1/49 duty), 1/6 (1/33 duty)
7. Read modify write: OFF
8. Static indicator: OFF
   Static indicator register: (D1, D2) = (0, 0)
9. The Display start line register is set at the first line.
10. The Column address counter is set at address 0.
11. The Page address register is set at page 0.
12. Common output status: normal
13. The V0 voltage regulator internal power supply ratio is reset to its default value.
    V0 voltage regulator internal resistor ratio register: (D2, D1, D0) = (1, 0, 0)
14. The Electronic volume register is reset to its default value.
    Electronic volume register: (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0,)
15. Resets during Test mode
16. Oscillation frequency: 31.4kHz
17. Normal display mode and frame inversion status (partial display and N-Line inversion release)
18. Partial display duty register: (D2, D1, D0) = (1, 0, 0), 1/65 duty
19. Partial display bias register: (D2, D1, D0) = (1, 0, 1), 1/9 bias
20. N-Line inversion register: (D4, D3, D2, D1, D0) = (0, 1, 1, 0, 0), 13-Line inversion
21. Partial start line register: (D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0), the first line
22. DC/DC clock division register: (D3, D2, D1, D0) = (0, 0, 1, 1), fOSC/6
23. Output condition of COM, SEG
    COM: VSS
    SEG: VSS

When the reset command is used, only default settings (7) to (15) listed above are executed.

The MPU interface, the RESB terminal is connected to the MPU reset terminal, making the chip reinitialize simultaneously with the MPU. During power on, it is necessary to reinitialize using the RESB terminal.

In the EM62100, if the internal liquid crystal power supply circuit is not used, it is necessary to apply an “L” signal to the RESB terminal when the external liquid crystal power supply is applied. Even though the oscillator circuit operates while the RESB terminal is “L”, the display timing generator circuit is stopped, and the M, FLM, and DOFB terminal is “H”, and the CKS terminal is fixed to “H” only when the internal oscillator circuit is used. There is no influence on D0 to D7 terminals.

7 Command Register & Decoder

The EM62100 uses a combination of A0, RDB (E), and WRB (RW) signals to identify the data bus signals. As the chip analyzes and executes each command using internal timing clock only, regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series MPU interface enters a read status when a low pulse is input to the RDB (E) pin and to a write status when a low pulse is input to the WRB (RW) pin. The 6800 series MPU interface enters a read status when a high pulse is input to the RW pin and to a write status when a low pulse is input to the RW pin. When there is a high pulse to the E pin, the command is activated. For timing details, see AC characteristics section.

Taking the 8080 series MCU interface as an example, the commands are explained below. Accordingly, in the command table and explanation, RDB (E) becomes high (1) when 6800 series MPU interface reads the display data status. When the serial interface is selected, the input data starts from D7 in sequence.

7.1 Command Table

Command	RS	RDB	WRB	Code									Function
				D7	D6	D5	D4	D3	D2	D1	D0	Hex	
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0 1	AEh AFh	Turns on the LCD panel when high, and turns off when low
(2) Display Start Line Set	0	1	0	0	1	Display Start Address						40h to 7Fh	Specifies the RAM display line for COM0
(3) Page Address Set	0	1	0	1	0	1	1	Page Address				B0h to B8h	Sets the display data RAM page in Page Address register
(4) Column Address Set	0	1	0	0	0	0	1	High Column Address				00h to 18h	Sets 4 higher bits and 4 lower bits of column address of display data RAM in register
	0	1	0	0	0	0	0	Low Column Address					
(5) Read Status	0	0	1	Status				0	0	0	0	XX	Reads the status information
(6) Write Display Data	1	1	0	Write Data								XX	Writes data in display data RAM
(7) Read Display Data	1	0	1	Read Data								XX	Reads data from display data RAM
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	A0h A1h	Sets the display data RAM address SEG output correspondence
(9) Normal/ Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	A6h A7h	Normal display when low, but reverse display when high
(10) Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	A4h A5h	Selects normal display (0) or entire display on
(11) LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0 1	A2h A3h	Sets the LCD driving voltage bias ratio
(12) Read-Modify -Write	0	1	0	1	1	1	0	0	0	0	0	E0h	Increments column address counter during each write

Command	RS	RDB	WRB	Code									Function
				D7	D6	D5	D4	D3	D2	D1	D0	Hex	
(13) End	0	1	0	1	1	1	0	1	1	1	0	EEh	Releases the Read-Modify-Write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	E2h	Resets internal functions
(15) Common Output Mode Select	0	1	0	1	1	0	0	0 1	*	*	*	C0h to CFh	Selects COM output scan direction
(16) Power Control Set	0	1	0	0	0	1	0	1	Operation Status			28h to 2Fh	Selects the power circuit operation mode
(17) V0 Voltage Regulator Internal Resistor Ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h to 27h	Selects internal resistor ratio Rb/Ra mode
(18) Electronic Volume Mode Set	0	1	0	1	0	0	0	0	0	0	1	81h	
Electronic Volume Register Set	0	1	0	*	*	Electronic Control Value						XX	Sets the V0 output voltage electronic volume register
(19) Set Static Indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	ACh ADh	Sets static indicator ON/OFF
Set Static Indicator Register	0	1	0	*	*	*	*	*	*	Mode		XX	Sets the flash mode
(20) Power Save	0	1	0	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation
(22) Oscillation Frequency Select	0	1	0	1	1	1	0	0	1	0	0 1	E4h E5h	Selects the oscillation frequency
(23) Partial Display Mode Set	0	1	0	1	0	0	0	0	0	1	0 1	82h 83h	Enter/Release the partial display mode
(24) Partial Display Duty Set	0	1	0	0	0	1	1	0	Duty Ratio			30h 37h	Sets the LCD duty ratio for partial display mode

Command	RS	RDB	WRB	Code									Function
				D7	D6	D5	D4	D3	D2	D1	D0	Hex	
(25) Partial Display Bias Set	0	1	0	0	0	1	1	1	Bias Ratio			38h 3Fh	Sets the LCD bias ratio for partial display mode
(26) Partial Start Line Set	0	1	0	1	1	0	1	0	0	1	1	D3h	Enters Partial Start Line Set
Partial Start Line	0	1	0	1	1	Partial Start Line						XX	Sets the LCD Number of partial display start line
(27) N-Line Inversion Set	0	1	0	1	0	0	0	0	1	0	1	85h	Enters N-line inversion
Number of Line Set	0	1	0	*	*	*	Number of Line					XX	Sets the number of line used for N-Line inversion
(28) N-Line Inversion Release	0	1	0	1	0	0	0	0	1	0	0	84h	Exits N-Line Inversion
(29) DC/DC Clock Set	0	1	0	1	1	0	0	0	1	1	0	E6h	Sets DC/DC Clock Frequency
DC/DC Clock Division Set	0	1	0	1	1	0	0	Clock Division				XX	Sets the Division of DC/DC Clock Frequency

Table 14

7.2 Command Function

7.2.1 Display ON/OFF

This command turns the display on or off. When display OFF command is executed during display all points ON mode, power saving mode is entered.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	1	1	1	1	AFH	Display ON
										0	AEH	Display OFF

7.2.2 Display Start Line Set

This command specifies a line address thus marking the display line that corresponds to COM0. When this command changes the line address, smooth scrolling or a page change occurs.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	1	A5	A4	A3	A2	A1	A0	40H to 7FH

D7	D6	D5	D4	D3	D2	D1	D0	40H to 7FH
0	1	A5	A4	A3	A2	A1	A0	Line Address
		0	0	0	0	0	0	0
		0	0	0	0	0	1	1
		0	0	0	0	1	0	2
					.			.
					.			.
					.			.
		1	1	1	1	1	0	62
		1	1	1	1	1	1	63

7.2.3 Page Address Set

This command is used to specify a page address equivalent to a row address for MPU access to the display data RAM. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 8 is the display RAM area indicated by the indicator, and only D0 is valid for data change.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	0	1	1	A3	A2	A1	A0	B0H to B8H

D7	D6	D5	D4	D3	D2	D1	D0	B0H to B8H
1	0	1	1	A3	A2	A1	A0	Page Address
				0	0	0	0	0
				0	0	0	1	1
				0	0	1	0	2
					.			.
					.			.
					.			.
				1	1	1	0	7
				1	0	0	0	8

7.2.4 Column Address Set

This command specifies a display data RAM column address. In setting, the column address is split into two parts (the upper 4-bits and the lower 4-bits). The column address is automatically incremented by 1 each time the MPU accesses from the set address to the display data RAM. Therefore, the MPU can access the data continuously. However, the column address is no longer incremented at address 131 (83H), and the page address is not changed continuously.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex	
0	1	0	0	0	0	1	A7	A6	A5	A4	10H to 18H	Upper bits
						0	A3	A2	A1	A0	00H to 0FH	Lower bits

A7	A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
					.			.
					.			.
					.			.
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

7.2.5 Read Status

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Busy: the busy bit indicates whether the driver accepts instruction or not.

Busy=0: the driver will accept new instruction

Busy=1: no new instruction will be accepted

ADC:

ADC=0: reverse (column address 131-n ↔ segment driver n)

ADC=1: normal (column address n ↔ segment driver n)

ON/OFF: indicates the current status of the display

ON/OFF=0: display ON

ON/OFF=1: display OFF

Reset: indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.

Reset=0: normal operation

Reset=1: currently executing a reset instruction

7.2.6 Write Display Data

Writes an 8-bit data from the data bus into the display RAM. Since the column address automatically increments by 1 after each write, the microprocessor can continue to write data with multiple words.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

7.2.7 Read Display Data

Reads an 8-bit data from the display RAM area specified by the column address and page address. Since the column address is automatically incremented by 1 after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after a column address setup. For details, refer to the display RAM section of the FUNCTIONAL DESCRIPTION. When serial interface is used, reading from the display data becomes invalid.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

7.2.8 ADC Select

Changes the relationship between the RAM column address and the segment driver. This command specifies the order of the segment driver pads. The column address is automatically incremented by 1 after every read or write operation is performed on the display data.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	0	0	0	0	A0H	Normal
										1	A1H	Reverse

7.2.9 Normal/Reverse Display

This command can reverse the lit and unlit display command without overwriting the contents of the display data RAM. After executing this command, the display data RAM contents are maintained.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	0	1	1	0	A6H	RAM data "H" LCD ON voltage (normal)
										1	A7H	RAM data "L" LCD ON voltage (reverse)

7.2.10 Entire Display ON

This command makes it possible to force all display points ON regardless of the contents of the display data RAM. The contents of the DISPLAY DATA RAM are maintained after executing this command. This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	0	1	1	0	A4H	Normal display mode
										1	A5H	Display all points ON

When D0 is high, the entire display ON status is provided. If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power saving mode. Refer to the Power Saving section for details.

7.2.11 LCD Bias Set

This command specifies the voltage Bias ratio for the LCD.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Duty			
												1/33	1/49	1/55	1/65
0	1	0	1	0	1	0	1	1	1	0	A2H	1/6bias	1/8bias	1/8bias	1/9bias
										1	A3H	1/5bias	1/6bias	1/6bias	1/7bias

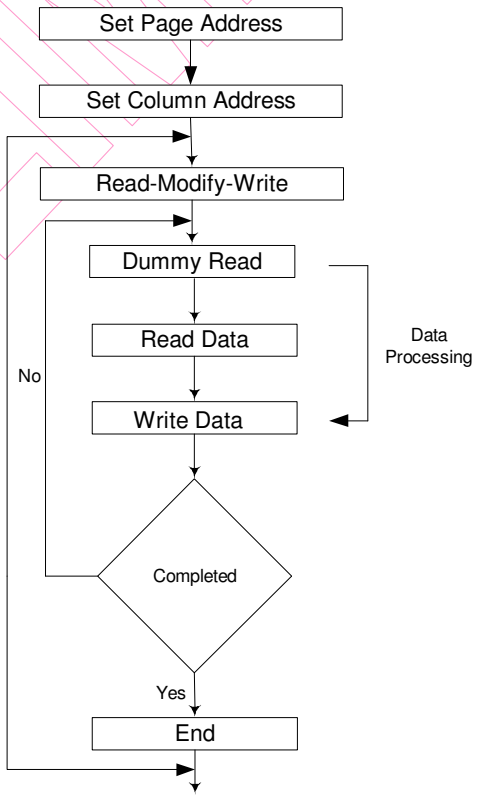
7.2.12 Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, the column address is not incremented by a Read Display Data command but incremented by a Write Display Data command only. The current contents of the column address register are saved. This mode remains active until an "End" command is issued, after which, the column address returns to the address when Read-Modify-Write command was issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or other events.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	0	0	0	0	E0H

NOTE

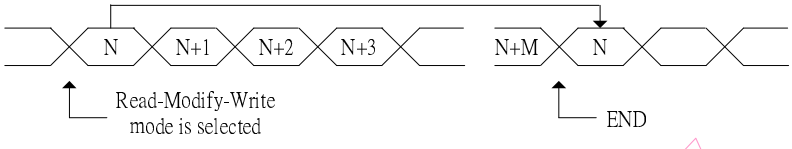
Any command except Read/Write Display Data and Column Address Set can be issued during Read-Modify-Write mode.



7.2.13 End

This instruction cancels the read-modify-write instruction, returning the column address to the initial mode address.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	1	1	1	0	EEH



7.2.14 Reset

This command initializes the Display Start Line register, the column address, the page address counter, and the Common output mode register, the V0 voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and read-modify-write mode and test mode are released. This does not affect the contents of the display RAM.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	0	0	1	0	E2H

The Reset command cannot initialize the LCD power supply. Only the Reset signal to the RESB pad can initialize the supplies.

7.2.15 Output Status Select Register

This command can select the scan direction of the common output terminal. When D3 is high or low, the scan direction of the COM output pad is selectable. For details, refer to the Output Status Selector Circuit in the FUNCTION DESCRIPTION section.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	0	0	0	*	*	*	C0H to C7H
							1				C8H to CFH

* Invalid bit

D3 = 0: Normal (COM0 → COM63/47/31)

D3 = 1: Reverse (COM63/47/31 → COM0)

7.2.16 Power Control Set

This command sets the function of the power supply circuit. Select one of the eight power circuit functions using a 3-bit register. An external power supply and part of an on-chip power circuit can be used simultaneously. For details, refer to the Power Supply Circuit in the FUNCTION DESCRIPTION section.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	1	0	1	VB	VR	VF	28H to 2FH

When VF goes low, the voltage follower turns off. When VF goes high, it turns on.

When VR goes low, the voltage regulator turns off. When VR goes high, it turns on.

When VB goes low, the voltage booster turns off. When VB goes high, it turns on.

7.2.17 V0 Voltage Regulator Internal Resistor Ratio Set

This command sets the V0 voltage regulator internal resistor ratio. For details, see the explanation under “The Power Supply Circuits”.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	0	0	1	0	0	0	0	0	20H	Small
								0	0	1	21H	
								0	1	0	22H	
									.		.	.
									.		.	.
									.		.	.
								1	1	0	26H	
								1	1	1	27H	Large

7.2.18 Electronic Volume (Double Byte Command)

This command allows adjustments can be made on the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is used in pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

(1) The Electronic Volume Mode Set

When this command is input, the electronic volume register set command is enabled. Immediately after the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	0	0	0	0	0	0	1	81H

(2) Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the LCD drive voltage V0 assumes one of the 64 voltage levels. When this command is input, the electronic volume mode is released after the electronic volume register has been set.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	*	*	0	0	0	0	0	1	01H	Small
					0	0	0	0	1	0	02H	
									.		.	.
									.		.	.
									.		.	.
					1	1	1	1	1	0	3EH	
					1	1	1	1	1	1	3FH	Large

When the electronic volume function is not used, set D5 - D0 to 100000.

7.2.19 Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands. This is used when one of the static indicator LCD drive electrodes is connected to the M terminal, and the other is connected to the FLM terminal. Different patterns are recommended for the static indicator electrodes and for the dynamic drive electrodes. If the patterns are too close, it can result in deterioration of the LCD and of the electrodes.

The static indicator ON command is a double bytes command paired with the static indicator register set command, and such commands must be executed one after the other. (The static indicator OFF command is a single byte command)

(1) Static Indicator ON/OFF

When the static indicator ON command is executed, the static indicator register set command is enabled, and no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	1	1	0	0	ACH	Static indicator OFF
										1	ADH	Static indicator ON

(2) Static Indicator Register Set

This command sets two bits of data into the static indicator register and used to set the static indicator into a blinking mode.

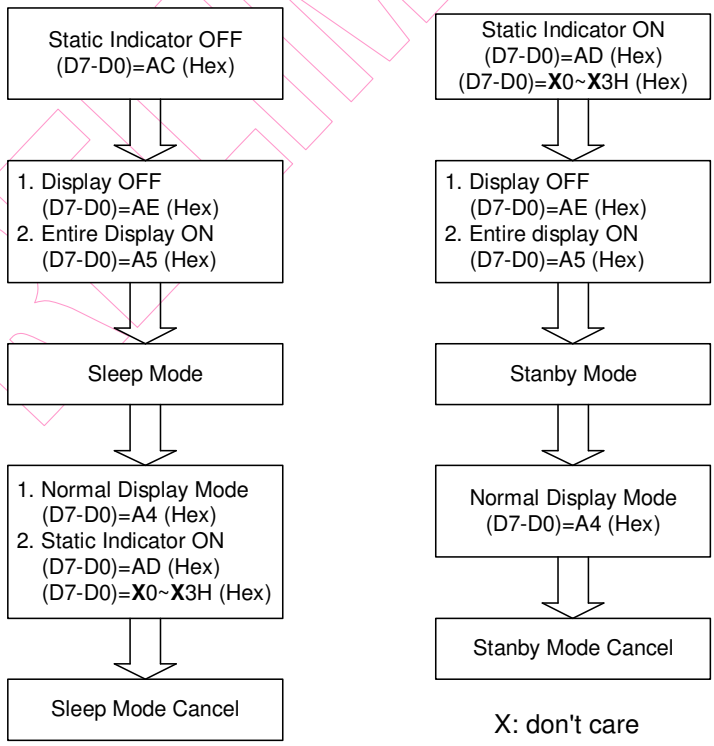
RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	*	*	*	*	*	*	0	0	00H	OFF
									0	1	01H	ON blinking at ≈ 1sec interval
									1	0	02H	ON blinking at ≈0.5sec interval
									1	1	03H	ON (constantly on)

7.2.20 Power Save (Compound Command)

The power save mode is entered when the display all points ON command is executed while in the display OFF mode. The power save mode includes the sleep mode and the standby mode. The sleep mode is entered when the static indicator is OFF, and the standby mode is entered when the static indicator is ON. This mode is cleared by the display all points OFF command.

The sleep mode operation stops all operations in the LCD display system, and as long as there are no accesses from the MPU. In sleep mode operation, the oscillator circuit, the LCD power supply circuit, and all LCD driver circuits are put on halt.

Release the Sleep mode using both Power Save OFF command (Display ON command or Entire Display OFF command) and Set Indicator On command.



X: don't care

Sleep Mode

This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

(1) Stops the oscillator circuit and LCD power supply circuit.

(2) Stops the LCD driver and outputs the VSS level as the segment/common driver output.

(3) Holds the display data and operation mode that momentarily existed before the start of the sleep mode.

(4) The MPU can access the built-in display data RAM.

Standby Mode

Stops the operation of the duty LCD display system and turns on only the static drive system to reduce power consumption to the minimum level required for static drive. The ON operation of the static drive system indicates that the EM62100 is in standby mode. The internal status in the standby mode is as follows:

(1) Stops the LCD power supply circuit.

(2) Stops the LCD drive and outputs the VSS level as the segment / common driver output. However, the static drive system still operates.

(3) Holds the display data and operation mode that momentarily existed before the start of the standby mode.

(4) The MPU can access the built-in display data RAM.

When the Reset command is issued in the standby mode, the sleep mode is set.

- When the LCD drive voltage level is provided by an external resistive driver, the current of this resistor must be cut so that it may be fixed to floating or VSS level, prior to or concurrently used, causing the EM62100 to go to the sleep mode or standby mode.
- When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to floating or VSS level, prior to or concurrently used, causing the EM62100 to go to the sleep mode or standby mode.

7.2.21 NOP

Non-Operation Command

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	0	0	1	1	E3H

7.2.22 Test Command

This is the dedicated IC chip test command. It must not be used during operation. It can be cleared by applying an "L" signal to set the RESB input or issue the reset command to release the test mode.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	1	0	1	0	0	F0H to FFH

7.2.23 Oscillation Frequency Select

This command is to select the oscillation frequency of the driver IC as shown below.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Oscillation Frequency
0	1	0	1	1	1	0	0	1	0	0	E4H	Typical 31.4kHz
										1	E5H	Typical 26.3kHz

7.2.24 Partial Display Mode Set

This command is to select the display mode. When D0 is "L", the IC is in normal display mode, the maximum display duty ratio is determined by the pin connection of DUTY0 and DUTY1 and the command LCD Bias Set determines the LCD bias ratio. The IC enters into partial display mode when D0 is high, then the commands Partial Display Duty Set and Partial Display Bias Set determine the LCD display duty and bias ratios.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Display Mode
0	1	0	1	0	0	0	0	0	1	0	82H	Normal Display
										1	83H	Partial Display

7.2.25 Partial Display Duty and Bias Set

These two commands set the LCD display duty and bias ratios when the IC is in partial display mode. Such commands are invalid when the IC is in normal display mode. When the partial display duty is set, the LCD bias for partial display is also set concurrently. The partial display duty will be kept at maximum duty (determine by pins DUTY0 and DUTY1) when the duty set is larger than the maximum duty.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Partial Duty	Scanning Line
0	1	0	0	0	1	1	0	0	0	0	30H	1/9 duty	Line[0:7], COMS
								0	0	1	31H	1/17 duty	Line[0:15], COMS
								0	1	0	32H	1/33 duty	Line[0:31], COMS
								0	1	1	33H	1/49 duty	Line[0:47], COMS
								1	0	0	34H	1/65 duty	Line[0:63], COMS
								1	0	1	35H	1/55 duty	Line[0:53], COMS
								1	1	*	36H/37H	Reserved	No effect

Using Partial Display Bias Set command to adjust the LCD bias in partial display mode.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex	LCD Bias
0	1	0	0	0	1	1	1	0	0	0	38H	1/4
								0	0	1	39H	1/5
								0	1	0	3AH	1/6
								0	1	1	3BH	1/7
								1	0	0	3CH	1/8
								1	0	1	3DH	1/9
								1	1	0	3EH	Reserved
								1	1	1	3FH	Reserved

NOTE

The COM waveform of no display area is non-select waveform.

7.2.26 Partial Start Line Set (Double Byte Command)

This command makes it possible to set the partial start line for partial display. It is a two-byte command used in pair and the Number of Start Line Set command must be issued after the Partial Start Line Set command.

(1) Partial Start Line Set

When this command is input, no other commands except for the Number of Start Line Set command can be used.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	0	1	0	0	1	1	D3H

(2) Number of Start Line Set

This command is used to set six bits of data to the Partial Start Line register. Immediately after the Number of Start Line Set command has been issued to set data into the register, then the partial start line will affect the LCD display. The number of partial start line is always equal to zero when the partial start line is larger than the maximum duty ratio (determine by pins DUTY0 and DUTY1).

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Partial Start Line
0	1	0	*	*	0	0	0	0	0	0	00H	0 line
					0	0	0	0	0	1	01H	1 line
					0	0	0	0	1	0	02H	2 lines
									.		.	.
									.		.	.
									.		.	.
					1	1	1	1	1	0	3EH	62 lines
					1	1	1	1	1	1	3FH	63 lines

7.2.27 N-line Inversion (Double Byte Command)

This command allows adjustments on the number of scan lines for liquid crystal display inversion. It is a two-byte command used in pair and the Number of Line Set command must be issued after the N-Line Inversion Set command.

7.2.27.1 N-Line Inversion Set

When this command is input, no other command except for the Number of Line Set command can be used.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	0	0	0	0	1	0	1	85H

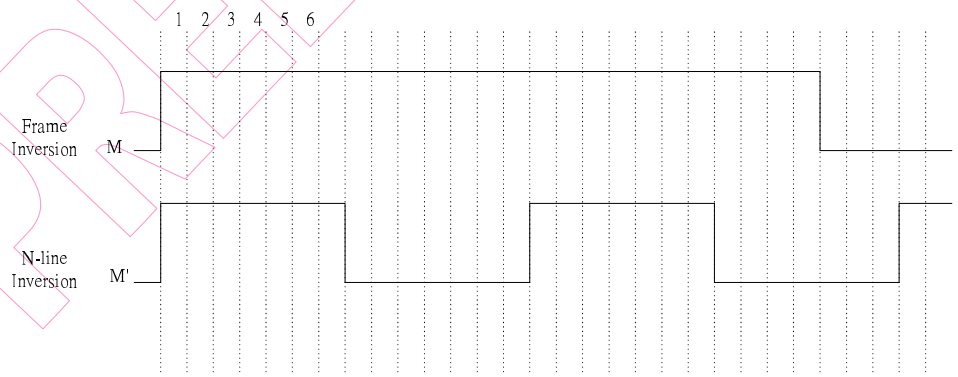
7.2.27.2 Number of Line Set

This command is used to set five bits of data to the N-Line inversion register. Once the Number of Line Set command has been issued to set data into the register, then the N-Line inversion will affect the LCD display.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Line Inversion
0	1	0	*	*	*	0	0	0	0	0	00H	1 line
						0	0	0	0	1	01H	2 lines
									.		.	.
						1	1	1	1	1	1FH	32 lines

NOTE

- *The number of inversed scan line = register setting value + 1.*
- *When Partial Duty = 1/9 or 1/17, the N-line inversion function is released and the LCD display scan line is back to frame inversion status.*



7.2.28 Release N-line Inversion

This command is used to cancel the N-Line inversion function. The N-Line inversion function is cancelled and the LCD display is set back to frame inversion status once this command is executed.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	0	0	0	0	1	0	0	84H

7.2.29 DC/DC Clock Frequency (Double Byte Command)

This command allows adjustments on the frequency for DC/DC clock. It is a two-byte command used in pair and the DC/DC Frequency Division Set command should be issued after the DC/DC Clock Set command.

7.2.29.1 DC/DC Clock Set

When this command is input, no other command except for the DC/DC Frequency Division Set command can be used.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	0	1	1	0	E6H

7.2.29.2 DC/DC Frequency Division Set

This command is used to set five bits of data to the frequency division register.

RS	RDB	WRB	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Division
0	1	0	*	*	*	*	0	0	0	0	00H	fOSC
							0	0	0	1	01H	fOSC/2
							0	0	1	0	02H	fOSC/4
							0	0	1	1	03H	fOSC/6
							0	1	0	0	04H	fOSC/8
							0	1	0	1	05H	fOSC/10
							0	1	1	0	06H	fOSC/12
							0	1	1	1	07H	fOSC/14
							1	0	0	0	08H	fOSC/16
							1	0	0	1	09H	fOSC/18
							1	0	1	0	0AH	fOSC/20
							1	0	1	1	0BH	fOSC/22
							1	1	0	0	0CH	fOSC/24
							1	1	0	1	0DH	fOSC/26
							1	1	1	0	0EH	fOSC/28
							1	1	1	1	0FH	fOSC/30

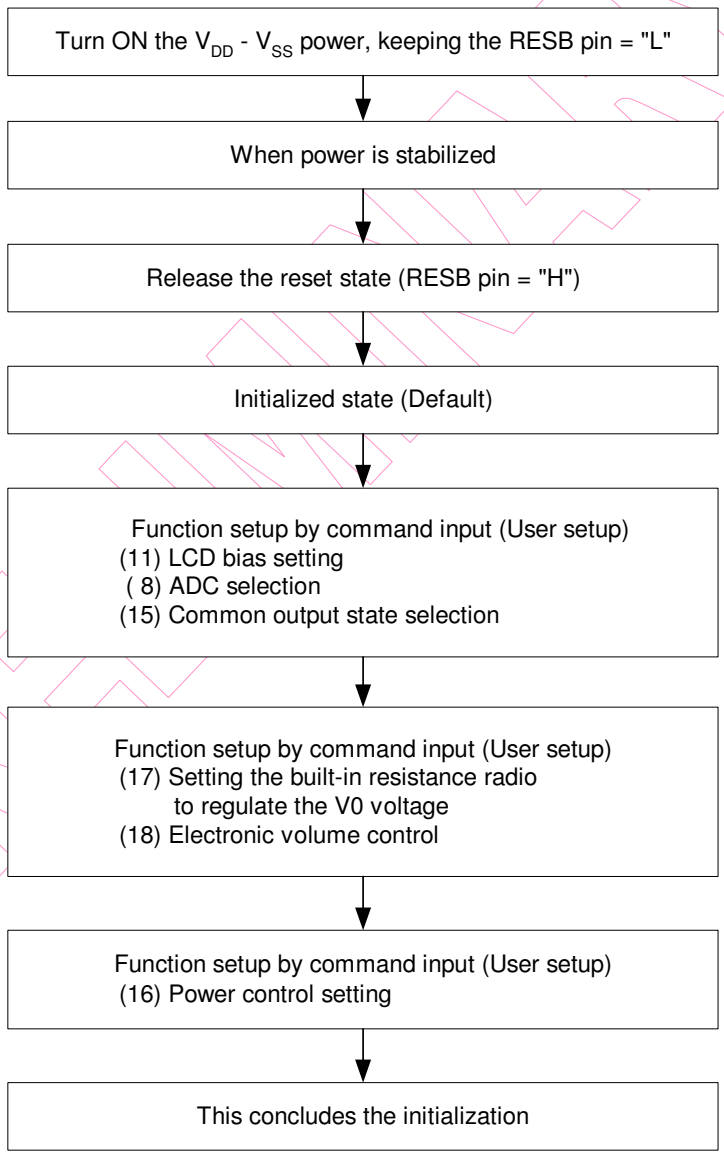
7.3 Chip Initial State and Power ON/OFF Flowchart:

7.3.1 Initialization

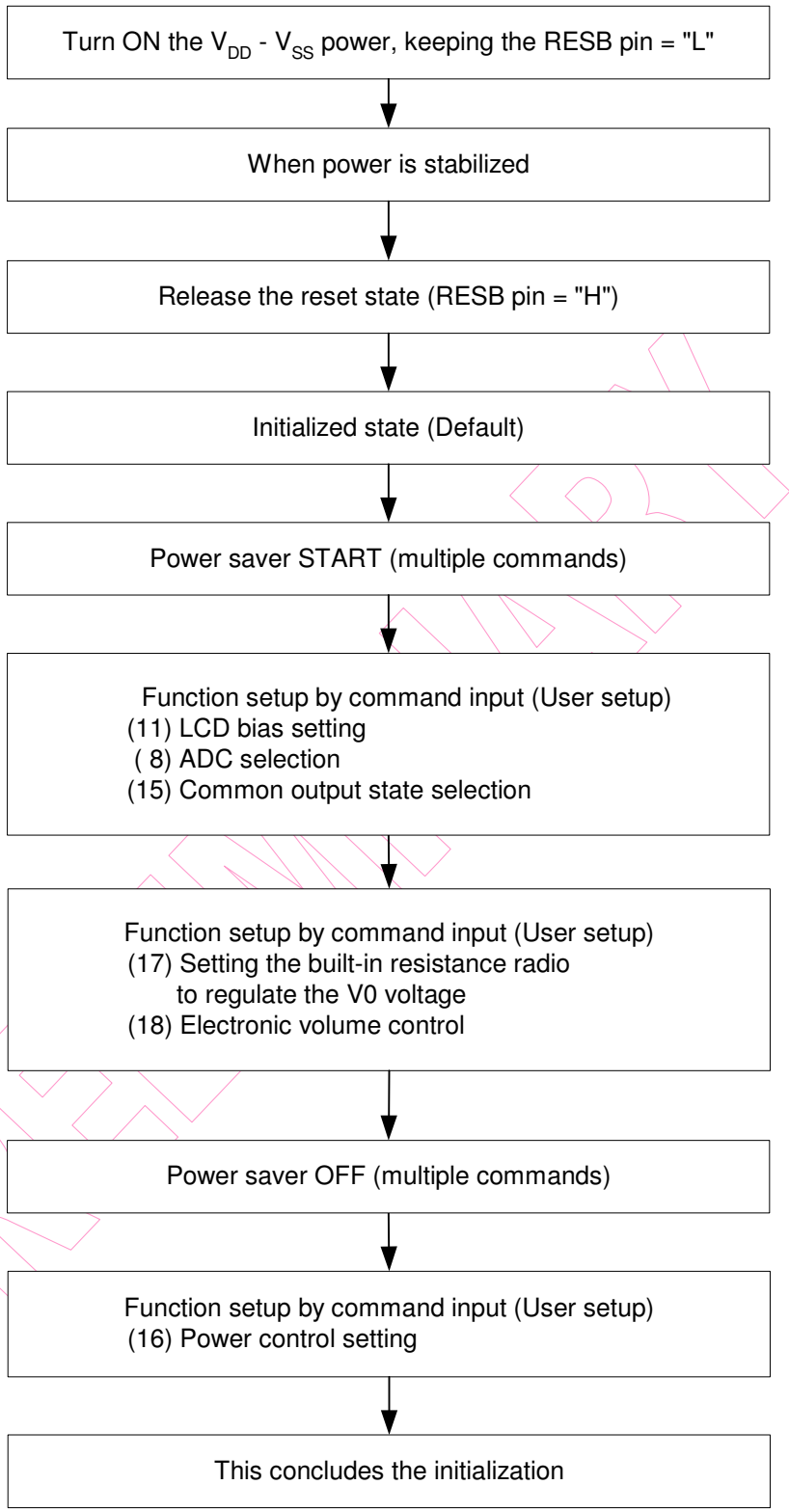
Note: For this chip, when power is applied, the LCD driving non-selective potentials V2 and V3 (segment pins) and V1 and V4 (common pins) are output through the LCD driving output pins SEG. and COM.

When electric charge still remains in the smoothing capacitor connecting between the LCD driving voltage output pins (V0 - V4) and the V_{DD} pin, the picture on the display may instantaneously become totally dark when power is turned on. To avoid such failure, we recommend the following flow sequence upon turning on the power.

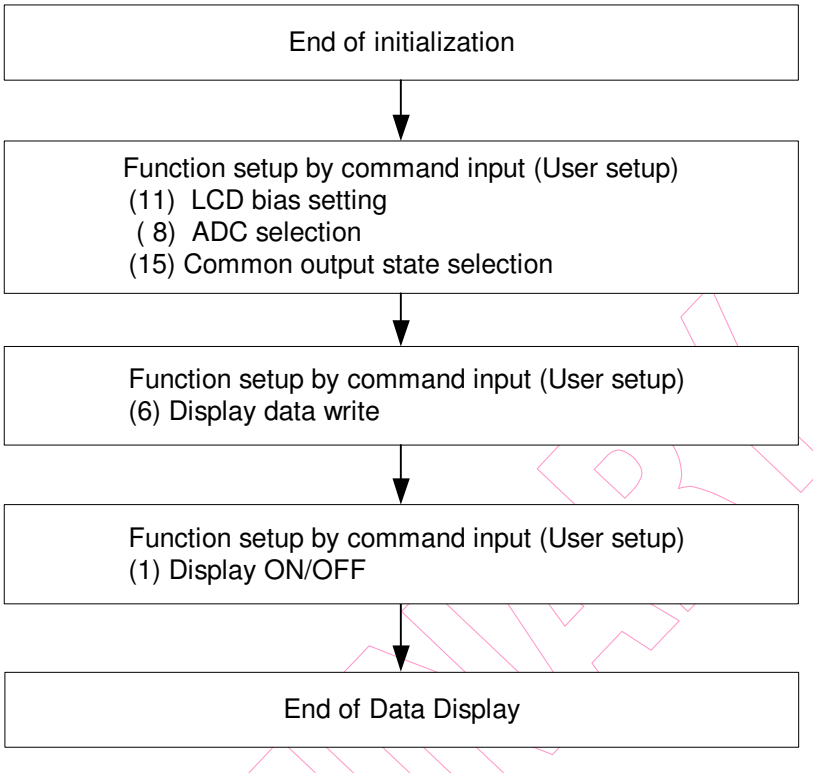
7.3.1.1 With instant built-in power supply circuit, after turning on the power



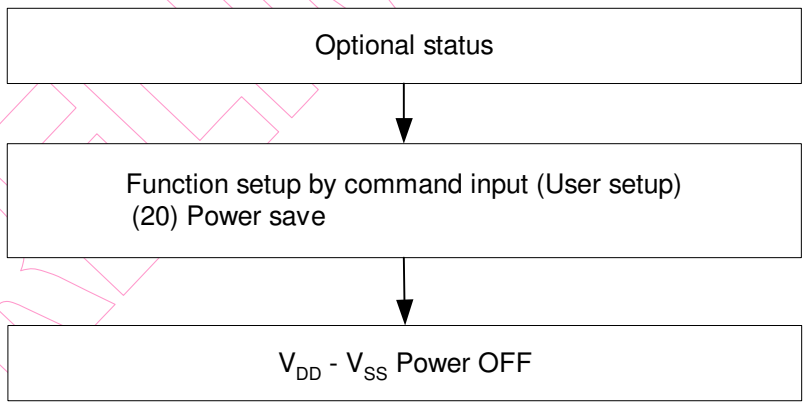
7.3.1.2 Without instant built-in power supply circuit, after turning on the power



7.3.1.3 Displaying Data



7.3.1.4 Power OFF



8 Absolute Maximum Ratings

Table 15 Absolute Maximum Ratings, unless otherwise specified, VSS = 0V

Parameter	Symbol	Conditions	
Power Supply Voltage	VDD ,V EE	–0.3 to +4.0	V
Power Supply Voltage	VOUT	-0.3 to +15.0	V
Power Supply Voltage	V0	-0.3 to +15.0	V
Input Voltage	VIN	–0.3 to VDD + 0.3	V
Operating Temperature	TOPR	–40 to +85	℃
Storage Temperature	TSTR	–55 to +125	℃

Notes and Cautions

1. Ensure that the voltage levels of V1, V2, V3, and V4 are such that they are always V0≥V1≥V2≥V3≥V4≥VSS.
2. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Hence, it is recommended that in normal operation the chip be used within the electrical characteristic conditions, otherwise, it may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

9 DC Characteristics

Table 16. DC Characteristics

Item	Symbol	Condition & Application Pin		Rating			Unit
				Min.	Typ.	Max.	
Operating Voltage (1)	VDD	Pin VDD		1.8	-	3.6	V
Operating Voltage (2)	V0			4.0	-	14.2	
High-level Input Voltage	VIHC	Pins RS, D0-D7, RDB (E), WRB (RW), CS1B, CS2, CKS, CK, M, M/S, M86, P/S, DOFB, RESB, IRS, HPMB		0.8xVDD		VDD	
Low-level Input Voltage	VILC			VSS		0.2xVDD	
High-level Output Voltage	VOHC	IOH=-0.5mA	Pins D0-D7, M , FLM, DOFB, CK	0.8xVDD		VDD	
Low-level Output Voltage	VOLC	IOL=0.5mA		VSS		0.2xVDD	
Input Leakage Current	ILI	VIN=VDD or VSS Pins RS, RDB (E), WRB (RW), CS1B, CS2, CKS, M/S, M86, P/S, RESB, IRS, HPMB		-1.0	-	1.0	µA
Hi-Z Leakage Current	IHZ	Pins D0-D7, M, FLM , DOFB, CK		-3.0	-	3.0	

Item	Symbol	Condition & Application Pin		Rating			Unit
				Min.	Typ.	Max.	
LCD Driver ON Resistor	RON1	Ta=25℃, Pin COMn & SEGn	V0=8V, |ΔV|=0.1V		2.0	3.5	kΩ
	RON2	Ta=25℃, Pin COMn & SEGn	V0=11V, |ΔV|=0.1V		3.2	5.4	
Sleep Mode Current Consumption	ISP	VDD= 3V, 4 times booster			0.01	5	μA
Standby Mode Current Consumption	ISB	VDD= 3V, 4 times booster			4	10	
Current Consumption	IDD1	VDD = 3V, V0=11V, built-in boosting power supply off, display on, display data = checker and no access, Ta=25℃		-	20	35	
	IDD2	VDD, VEE = 3V, V0=11V, 4X built-in boosting power supply, display on, display data = checker and no access, temperature gradient is -0.05% ℃, Ta=25℃, V0 voltage internal resistor is used, HPMB = 1 (normal power mode)		-	90	160	
	IDD3	VDD, VEE = 3V, V0=11V, 4X built-in boosting power supply, display on, display data = checker and no access, temperature gradient is -0.05% ℃, Ta=25℃, V0 voltage internal resistor is used, HPMB = 0 (high power mode)		-	150	255	
Input Terminal Capacitance	CIN	Ta=25℃, f=1MHz		-	5.0	8.0	pF
Frame Frequency	fFRM	fOSC = 31.4kHz, 1/65 duty VDD = 1.8~3.6V		78.1	80.5	82.9	Hz
		fOSC = 26.3kHz, 1/65 duty VDD = 1.8~3.6V		65.4	67.4	69.5	
Input Voltage	VEE	With twice boost ratio		1.8	-	3.6	V
		With triple times boost ratio		1.8	-	3.3	
		With quad and five times boost ratio		1.8	-	3.0	

Item	Symbol	Condition & Application Pin	Rating			Unit
			Min.	Typ.	Max.	
Supply Step-up Output Voltage	VOUT1	Booster output voltage on VOUT pin (x5)	5xVEE x0.95	5xVEE x0.98	5xVEE	V
	VOUT2	Booster output voltage on VOUT pin (x4)	4xVEE x0.95	4xVEE x0.98	4xVEE	
	VOUT3	Booster output voltage on VOUT pin (x3)	3xVEE x0.95	3xVEE x0.98	3xVEE	
	VOUT4	Booster output voltage on VOUT pin (x2)	2xVEE x0.95	2xVEE x0.98	2xVEE	
Base Voltage	VREG	Ta=25℃	2.04	2.10	2.16	V

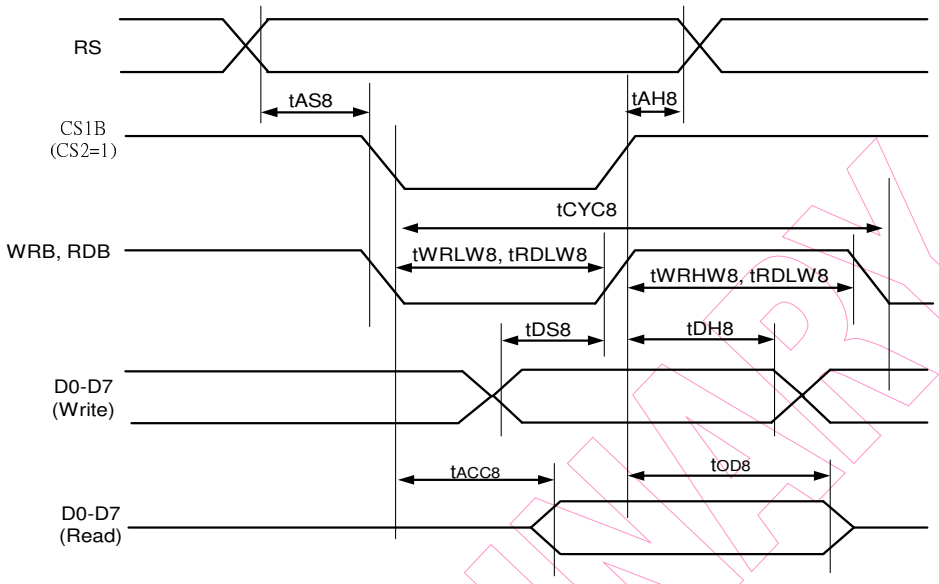
NOTE

1. Ensure that the voltage levels of V1, V2, V3, and V4 are in such a way that V0≥V1≥V2≥V3≥V4≥VSS.

2. Unless otherwise specified, VSS = 0V, VDD = 1.8 - 3.6V ±10%, Ta = –40 to 85℃

10 Timing Diagram

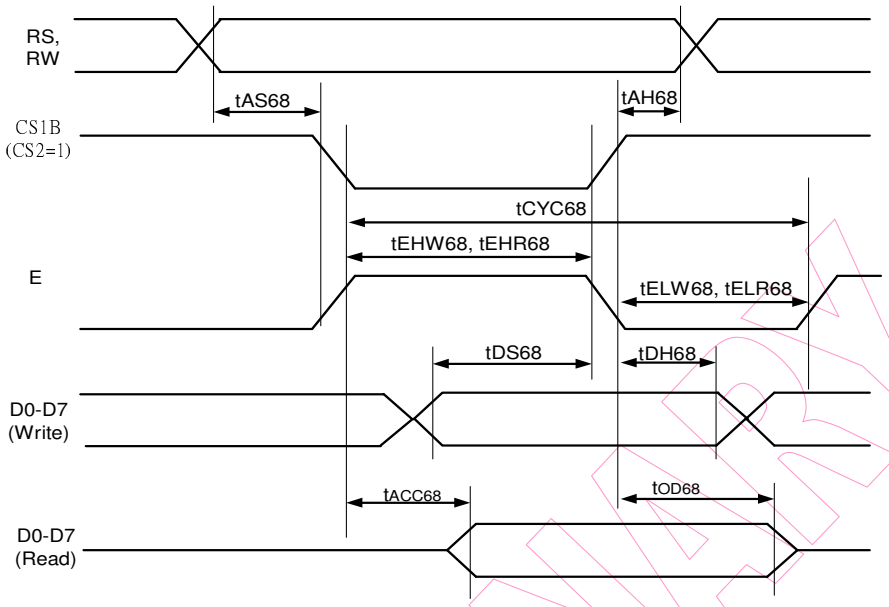
10.1 System Bus Read/Write Characteristics (8080-Series Microprocessor)



(VDD = 2.7 ~ 3.6V, Ta = -40~+85℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address Hold time	tAH8		0			ns	RS
Address Setup Time	tAS8		0			ns	
System Cycle Time	tCYC8		240			ns	WRB (RW)
Write Pulse “L” Width	tWRLW8		120			ns	
Write Pulse “H” Width	tWRHW8		100			ns	
Data Setup Time	tDS8		40			ns	D0-D7
Data Hold Time	tDH8		10			ns	
Read Pulse “L” Width	tRDLW8		120			ns	RDB (E)
Read Pulse “H” Width	tRDHW8		100			ns	
RDB Access Time	tACC8	CL = 100 pF			140	ns	D0-D7
Output Disable Time	tOD8		5		50	ns	

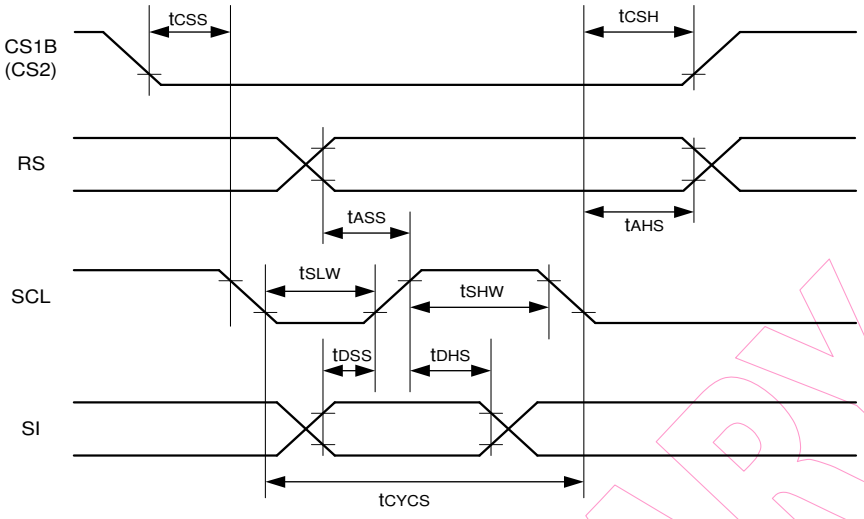
10.2 System Bus Read/Write Characteristics (6800-Series Microprocessor)



VDD = 2.7 ~ 3.6V, Ta = -40~+85℃

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Address Hold Time	tAH68		0			ns	RS, RW
Address Setup Time	tAS68		0			ns	
System Cycle Time (Write)	tCYC68		240			ns	
Enable pulse “H” Width (Write)	tEHW68		120			ns	E
Enable Pulse “H” Width (Read)	tEHR68		120			ns	
Enable Pulse “L” Width (Write)	tELW68		100			ns	
Enable Pulse “L” Width (Read)	tELR68		100			ns	
Data Setup Time	tDS68		40			ns	D0~D15
Data Hold Time	tDH68		10			ns	
RDB Access Time	tACC68	CL = 100 pF			140	ns	D0-D7
Output Disable Time	tOD68		5		50	ns	

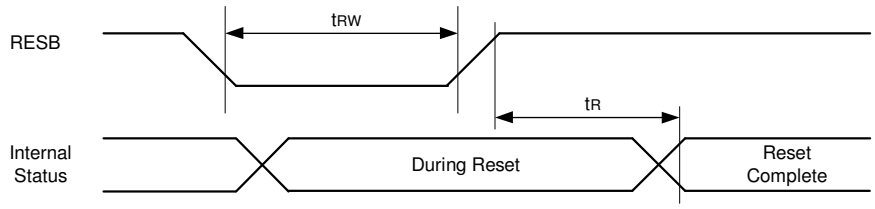
10.3 Serial Interface Characteristics



VDD = 2.7~3.6V, Ta = -40~+85℃ . In serial mode, keep M86=L, RDB=H, WRB=H.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Serial Clock Period	tCYCS		120			ns	SCL
SCL Pulse “H” Width	tSHW		60			ns	
SCL Pulse “L” Width	tSLW		60			ns	
Address Setup Time	tASS		30			ns	RS
Address Hold Time	tAHS		20			ns	
Data Setup Time	tDSS		30			ns	SI
Data Hold Time	tDHS		20			ns	
CSB-SCL Time	tCSS		20			ns	CSB, CS2
CSB Hold Time	tCSH		40			ns	

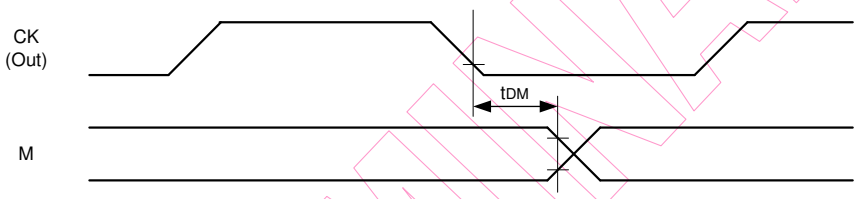
10.4 Reset Timing



VDD = 2.7~3.6V , Ta = -40~+85℃

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Reset Time	tR				1	µs	-
Reset Low Pulse Width	tRW		10			µs	RESB

10.5 Display Control Timing



VDD = 2.7~3.6V , Ta = -40~+85℃

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
M Delay Time	tDM	CL=50pF		20	80	ns	M

10.6 Application Circuit

The MPU Interface (Reference Example)

The EM62100 can be connected to either 80-Series MPU or 68-Series MPU. Using the serial interface makes it possible to operate the EM62100 series chips with fewer signal lines. The display area can be enlarged by integrating several EM62100 Series chips, after which, the chip select signal can be used to select the individual ICs to access.

10.6.1 8080-Series MPU

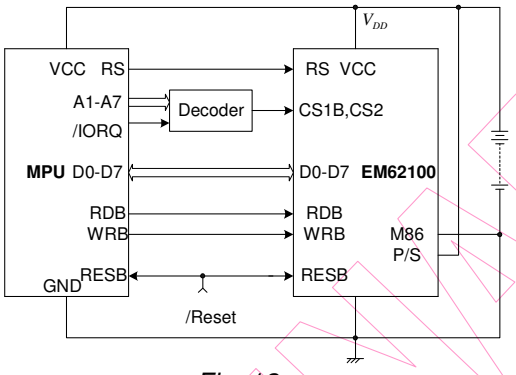


Fig. 12

10.6.2 6800-Series MPU

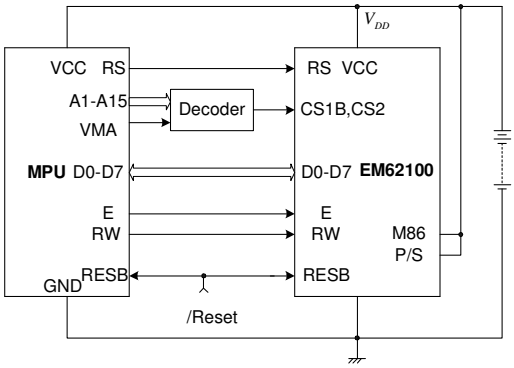


Fig. 13

10.6.3 Using the Serial Interface

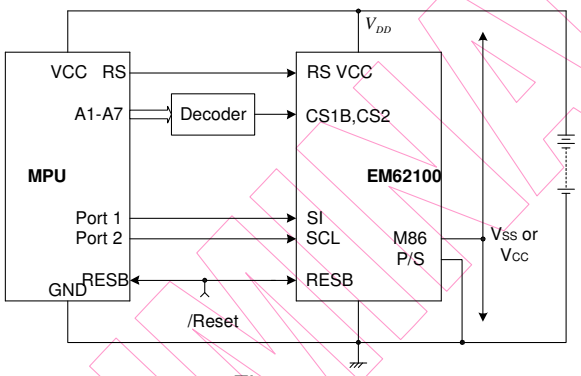


Fig. 14